PHASE II Cadence
Table of contents

Cadence Parameters

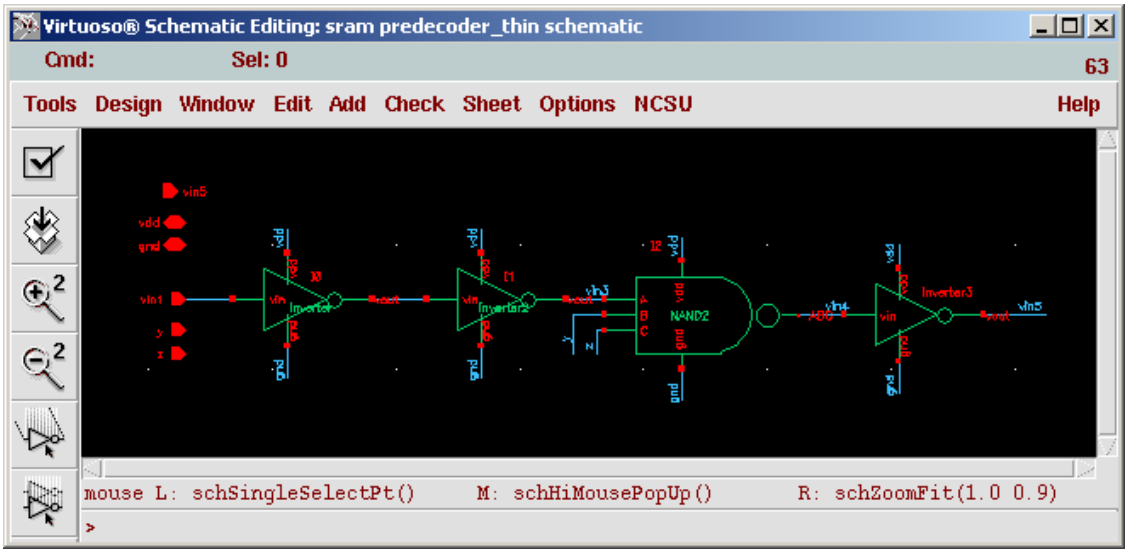
The widths for PMOS and NMOS are listed below.
pwidth = 0.7200 2.64 1.5 5.4 1.44 5.34
nwidth = 0.3600 1.32 2.22 2.7 2.16 2.64

Final Parameters after Resizing for 3 (or 2) Multipliers.

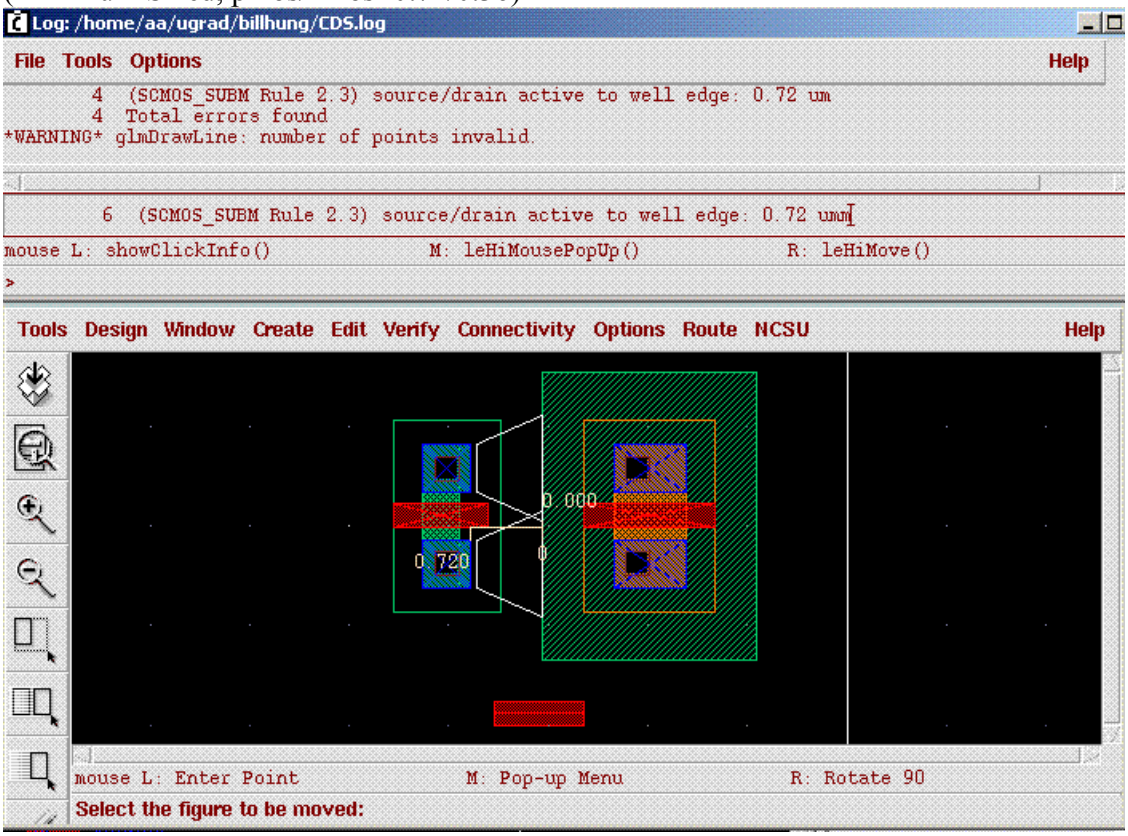
pmos
0.72 2.64 1.5 5.4 1.44 5.40
nmos
0.36 1.32 2.22 2.76 2.16 2.70

Cadence Layout

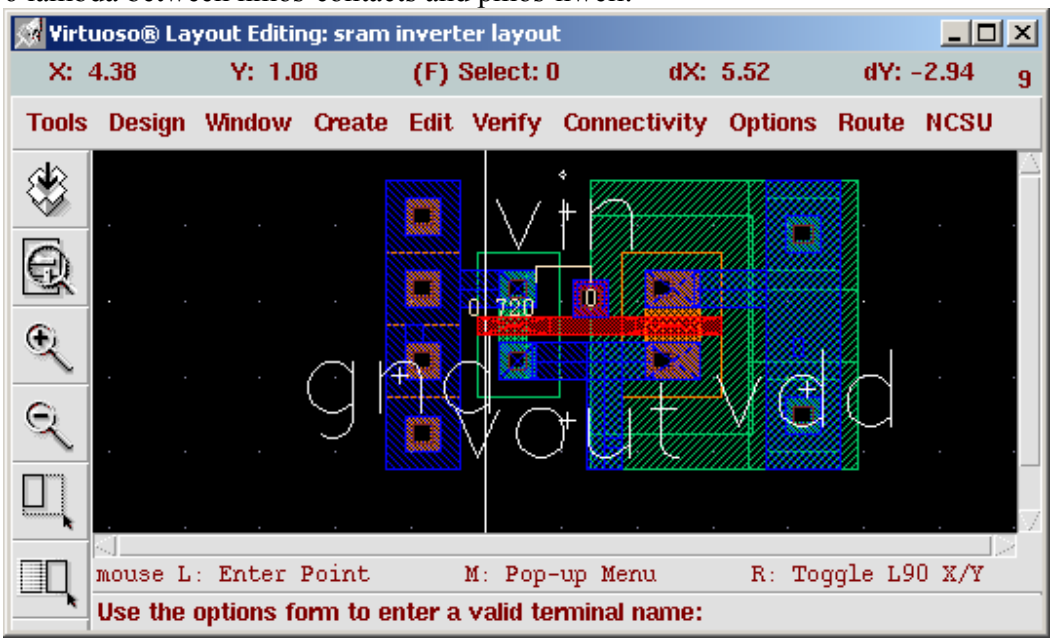
The goal of this part is to built a decoder with the logic of not-not-nand-not-nand-not. The first 3-input-nand gate has a branch factor of 4, and the second 3-input-nand gate has a branch factor of 8.



Inverter 1 – First Inverter
(Minimum Sized, pmos/nmos=0.72/0.36)



6 lambda between nmos-contacts and pmos-nwell.



Testing LVS with minimum sized inverter.
DRC -> Total errors found: 0
Extract -> Total errors found: 0

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

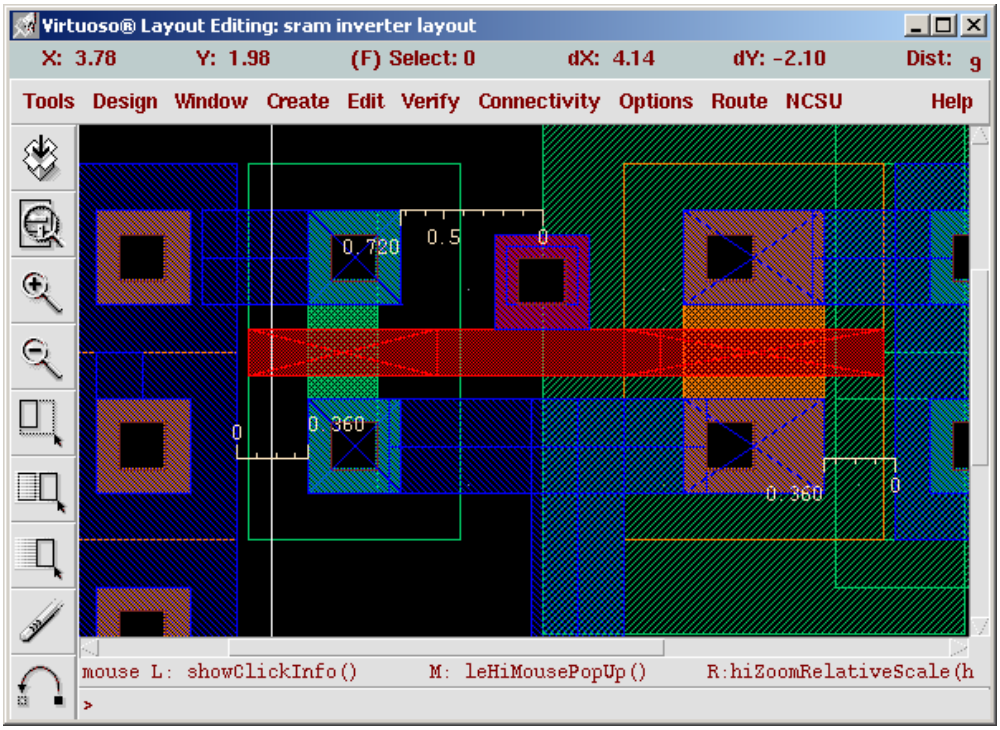
count	
4	nets
4	terminals
1	pmos
1	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

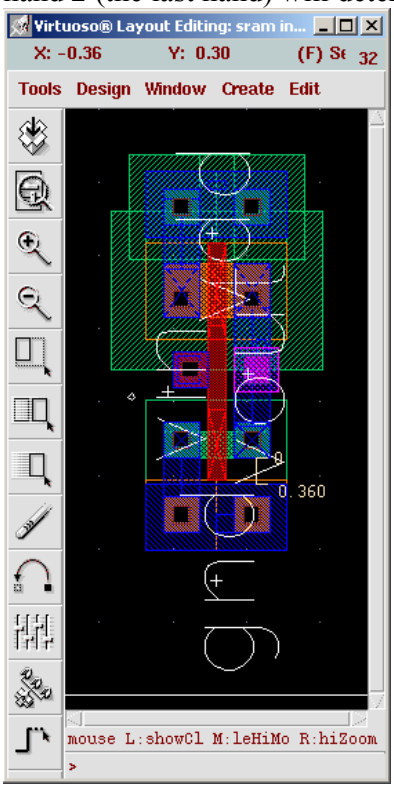
count	
4	nets
4	terminals
1	pmos
1	nmos

The net-lists match.
LVS->Pass **GREAT**

Minimize the size of Inverter 1



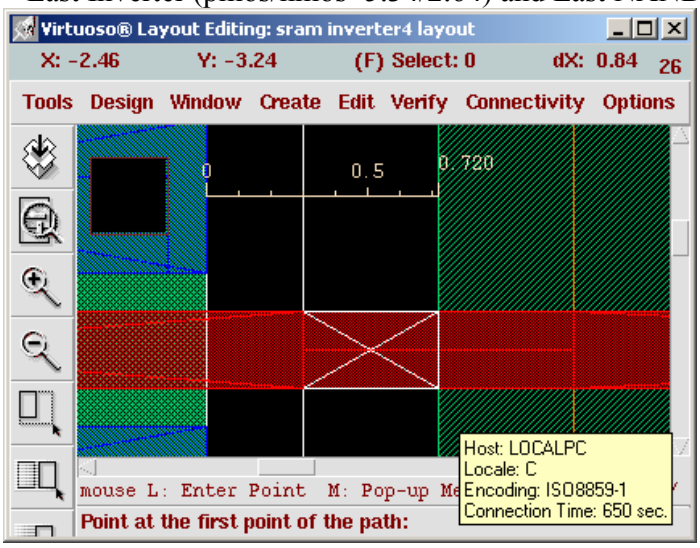
metal1=3 lambda, nmos-contact to pmos-nwell=6 lambda. The ntaps and ptaps are currently placed on the left and right sides. The inverter 4 (the biggest one) and 3-input nand 2 (the last nand) will determine the locations of the ntap and ptap.



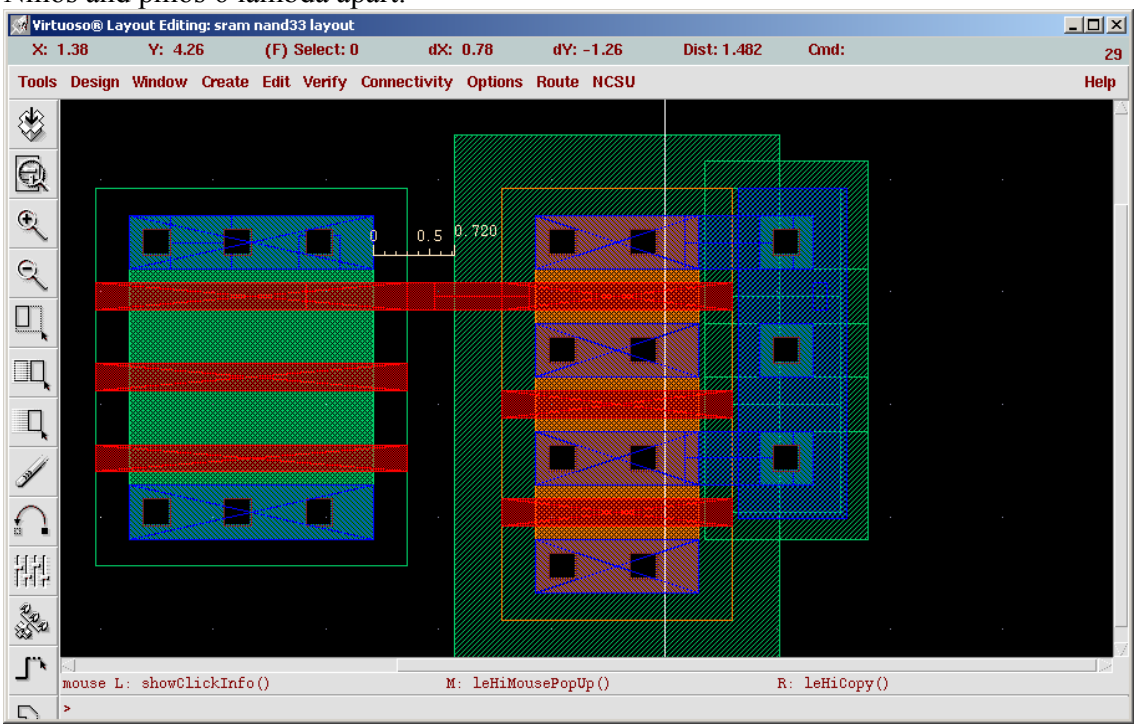
Inverter 1 final layout

Inverter 4 and 3-input-NAND

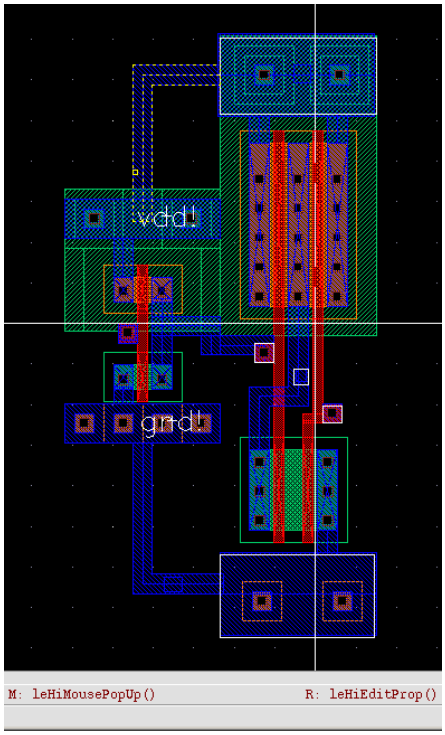
– Last Inverter (pmos/nmos=5.34/2.64) and Last NAND (pmos/nmos=1.44/2.16)



Nmos and pmos 6 lambda apart.



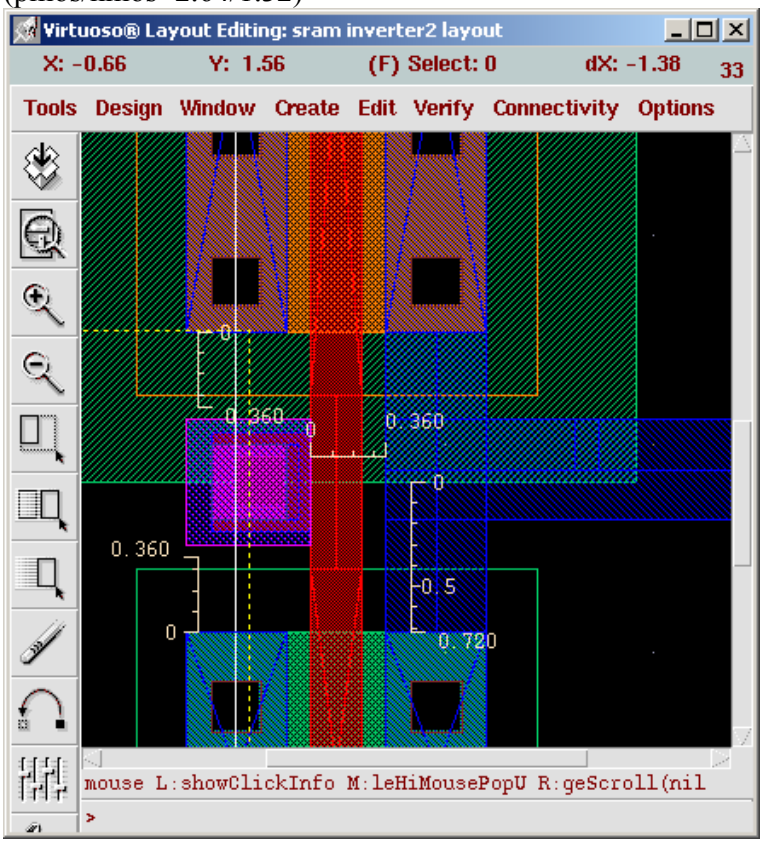
Last 3-input-NAND Gate



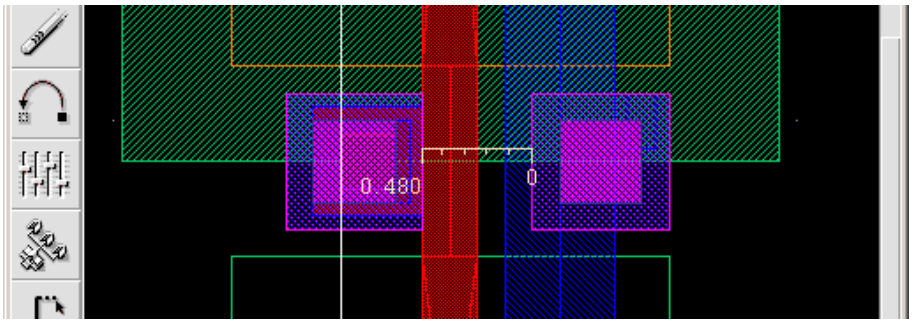
2-input NAND Gate

Inverter 2

(pmos/nmos=2.64/1.32)



Adding M1-M2 contact, 3 lambda metal1 spacing, 6 lambda pmos-nmos spacing.



Metal2 spacing 4 lambda.

LVS Results

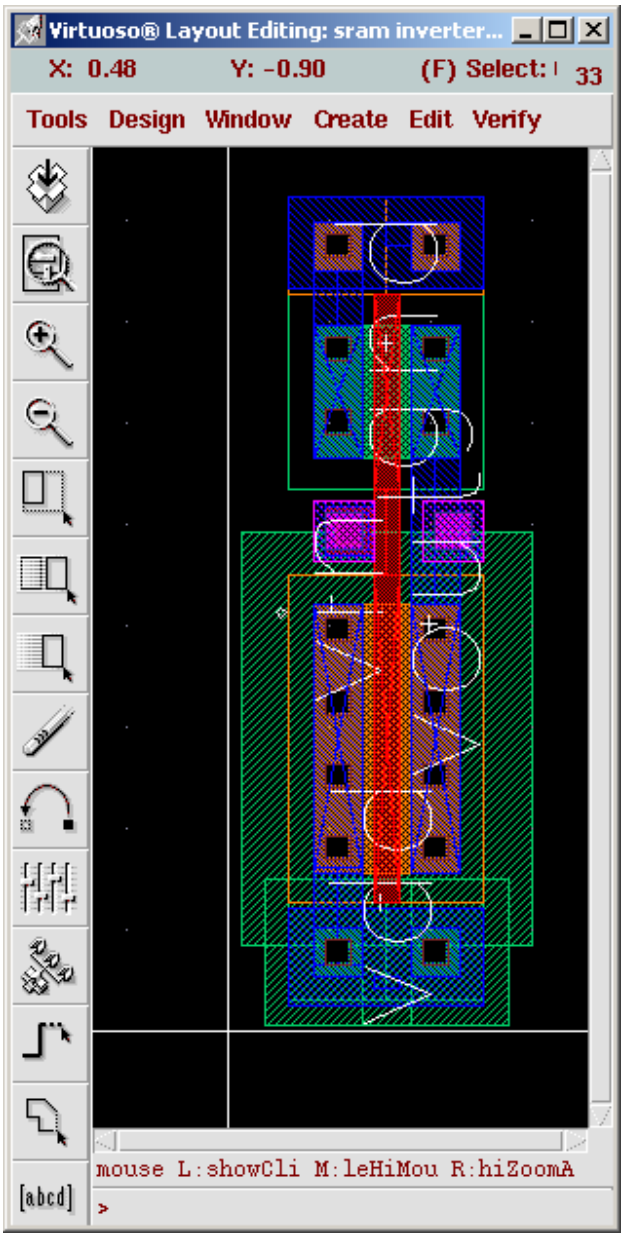
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

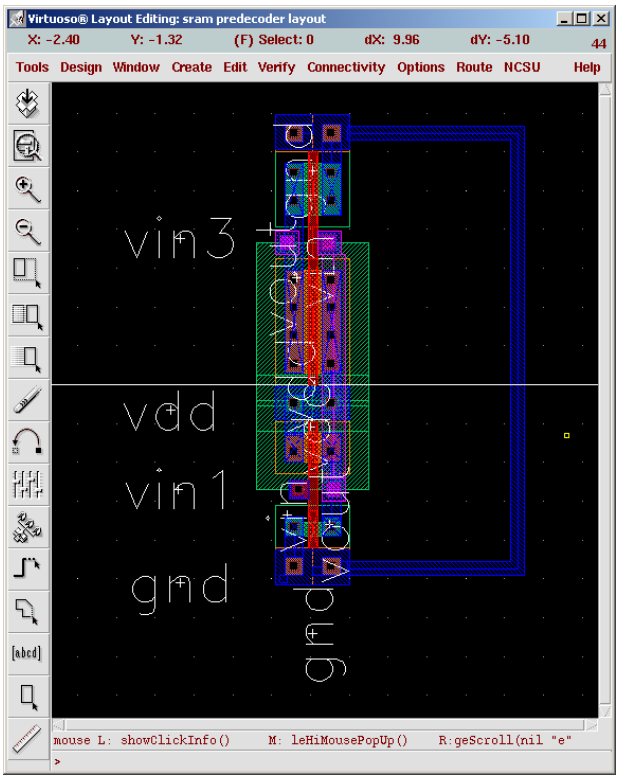
count	
4	nets
4	terminals
1	pmos
1	nmos

The net-lists match.

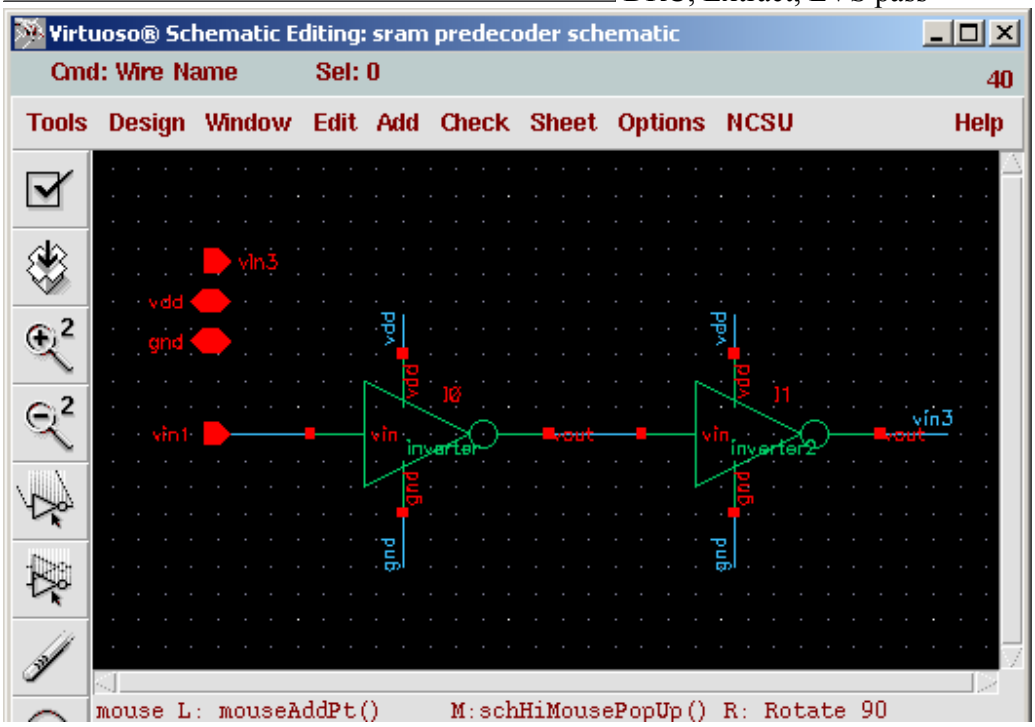


Inverter 2 final layout. The cell was flipped to share the vdd and gnd.

Inverter1 + Inverter 2



DRC, Extract, LVS pass

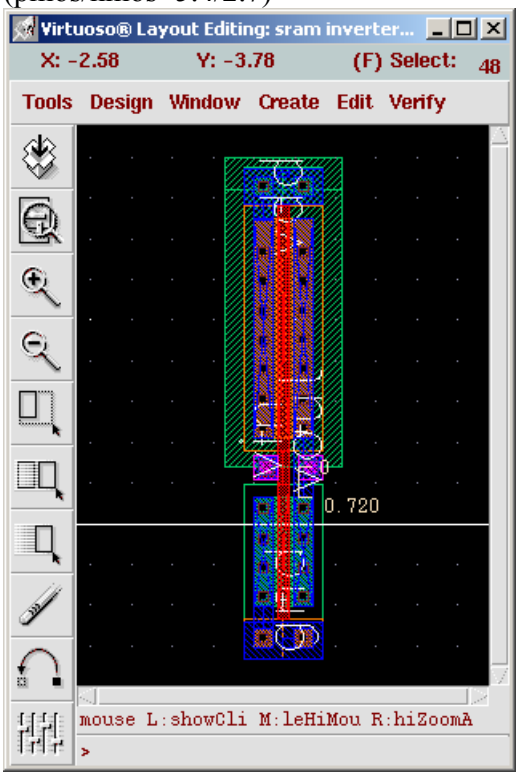


LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist
count
4 nets
4 terminals
1 pmos
1 nmos
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist
count
4 nets
4 terminals
1 pmos
1 nmos
The net-lists match.

Inverter 3

(pmos/nmos=5.4/2.7)



DRC, Extract, LVS Pass

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

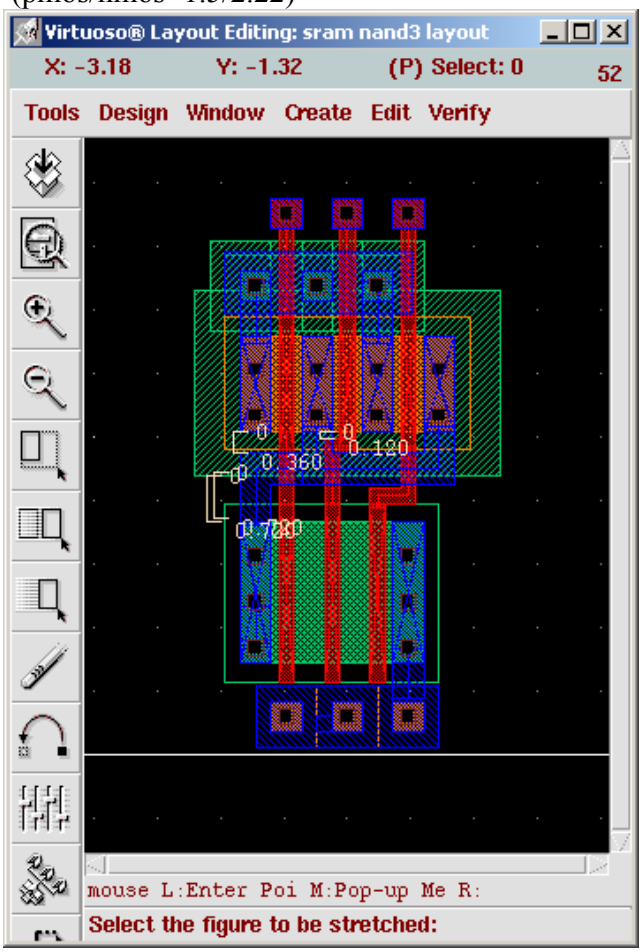
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

The net-lists match.

Predecoder NAND

(pmos/nmos=1.5/2.22)



3-input NAND

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
10	nets
6	terminals
5	pmos
5	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
10	nets
6	terminals
5	pmos
5	nmos

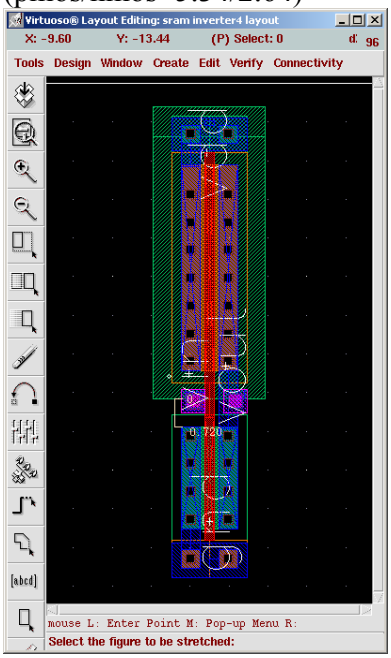
Terminal correspondence points

1	gnd
2	vdd
3	vin1
4	vin4
5	y
6	z

The net-lists match.

Inverter 4

(pmos/nmos=5.34/2.64)



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

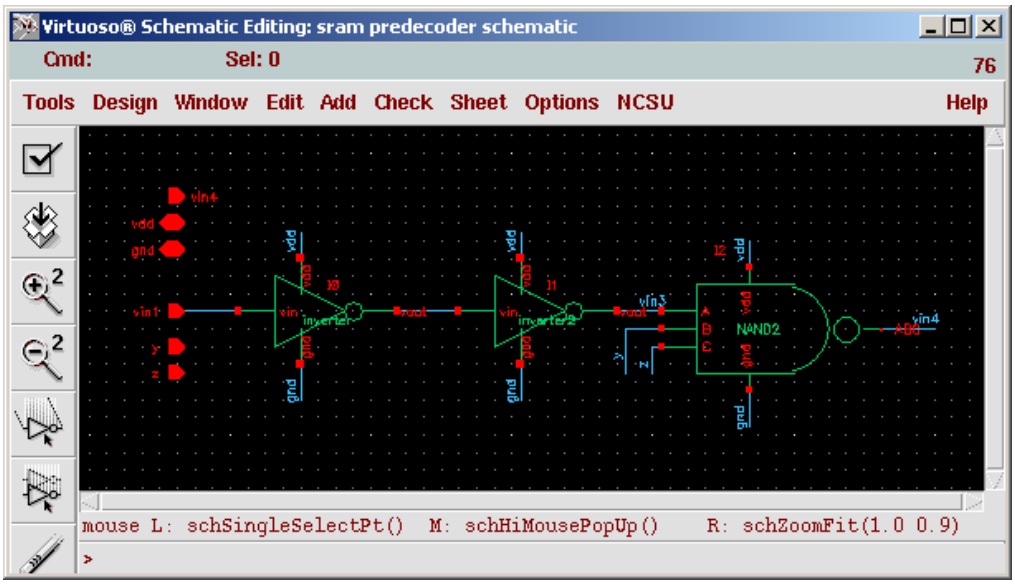
count	
4	nets
4	terminals
1	pmos
1	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

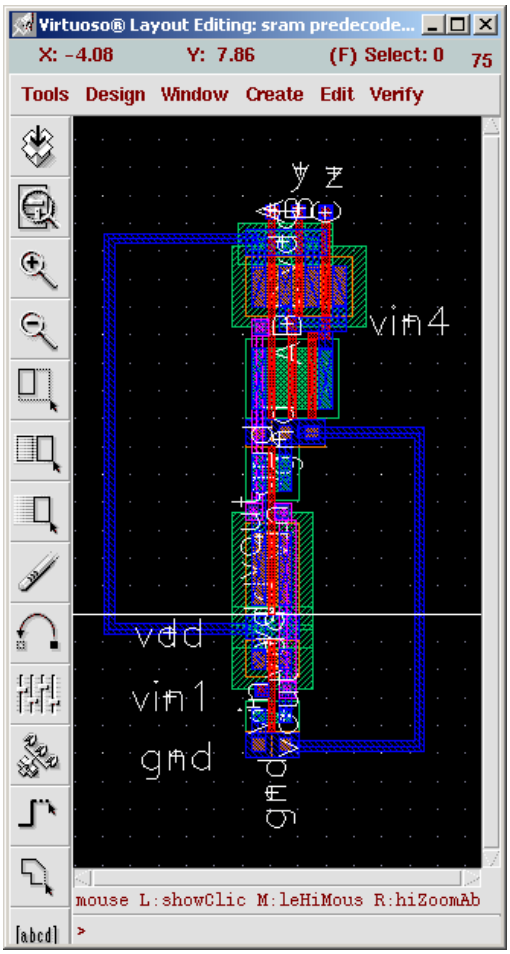
count	
4	nets
4	terminals
1	pmos
1	nmos

The net-lists match.

Inverter1 + Inverter 2 + Predecoder NAND



Schematic



Final Layout

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
10	nets
6	terminals
5	pmos
5	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

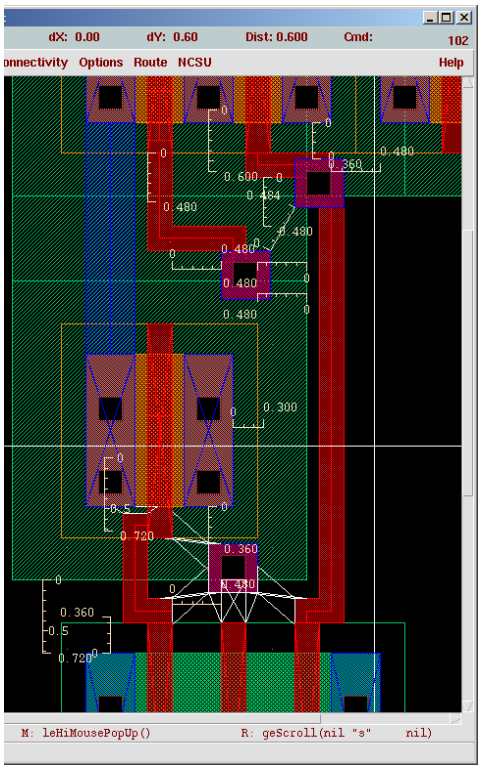
count	
10	nets
6	terminals
5	pmos
5	nmos

Terminal correspondence points

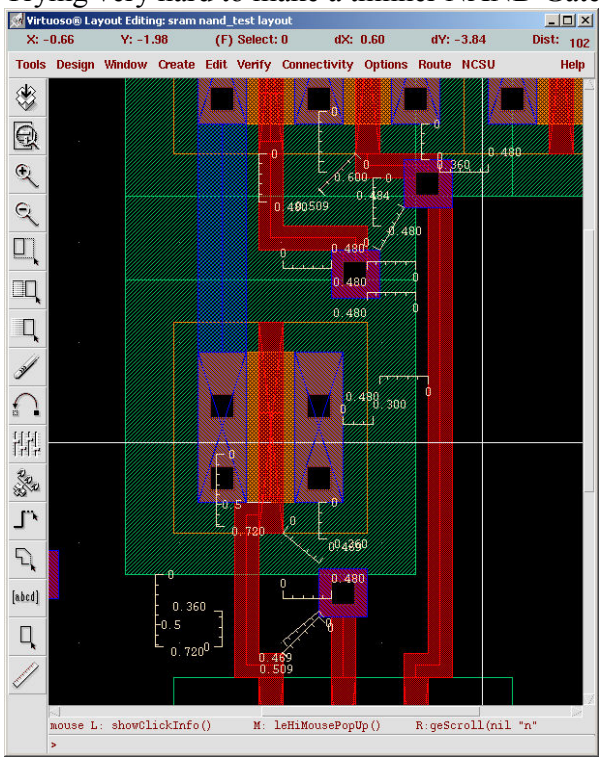
1	gnd
2	vdd
3	vin1
4	vin4
5	y
6	z

The net-lists match.

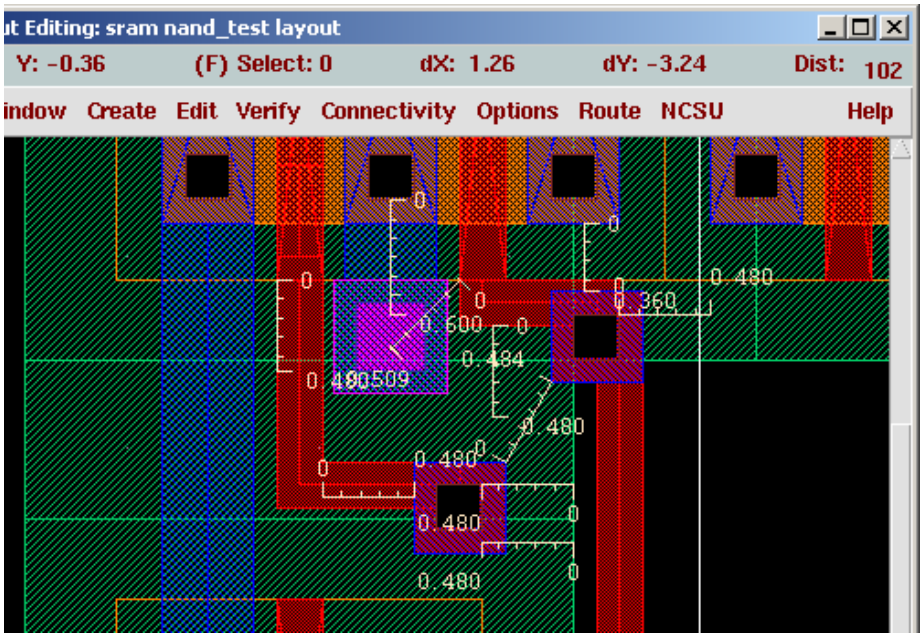
Thinner 3-input NAND



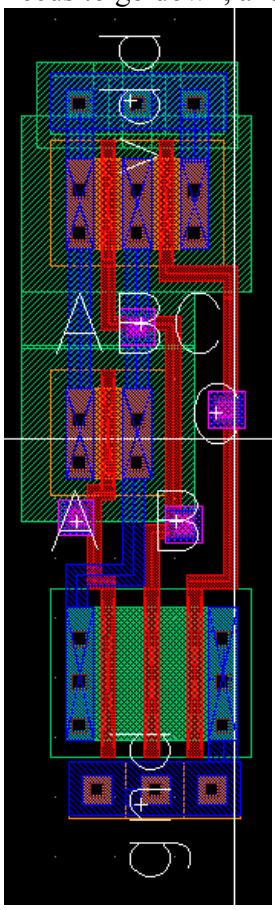
Trying very hard to make a thinner NAND Gate



Getting with some wiring troubles



The M1_M2 contact placed here has no DRC error, but the M2 from the output contact needs to go down, and the contact from the poly wants to go down. So this won't work.



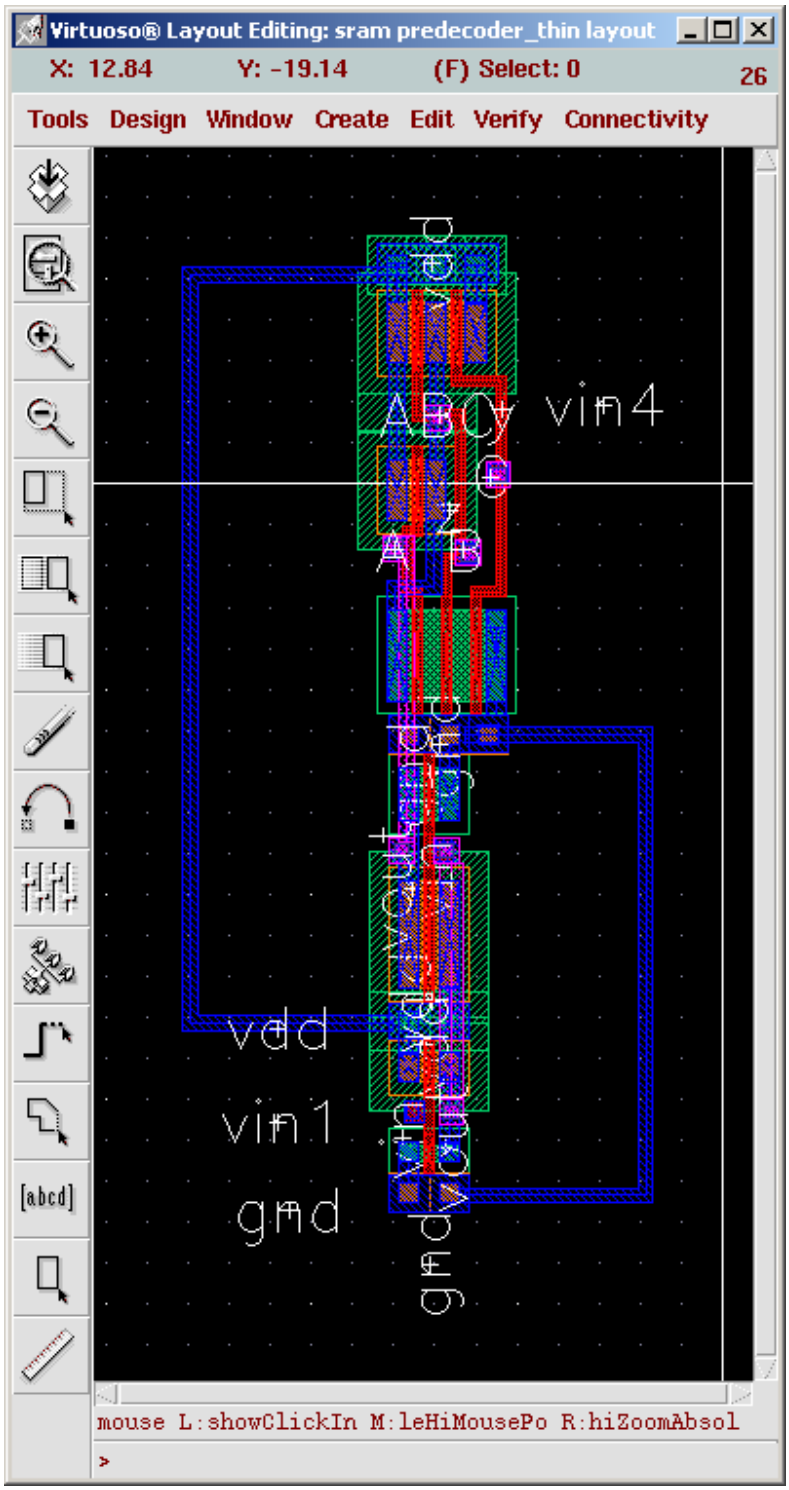
Final Thinner 3-input NAND Gate

Before-> Horizontal=3.30um, vertical=6.78um
Now-> Horizontal=3.12 um , vertical=11.46umz

Fat NAND versus Thin NAND
176.94um^2 versus 87.984um^2
Thin NAND won

Calculation
Fat
6*(3.36-2.88)*1.92*32 = 176.94
Thin
2.88*6*(11.48-6.78) = 87.984

Inverter1 + Inverter 2 + Thin Predecoder NAND



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
8	nets
6	terminals
3	pmos
3	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

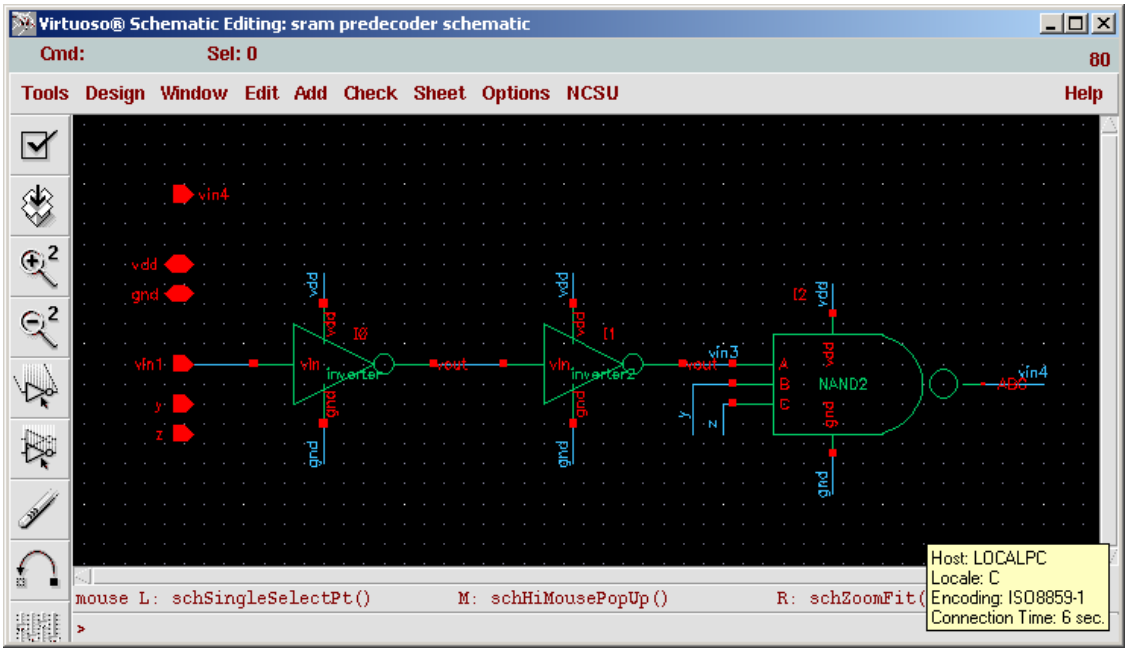
count	
8	nets
6	terminals
3	pmos
3	nmos

Terminal correspondence points

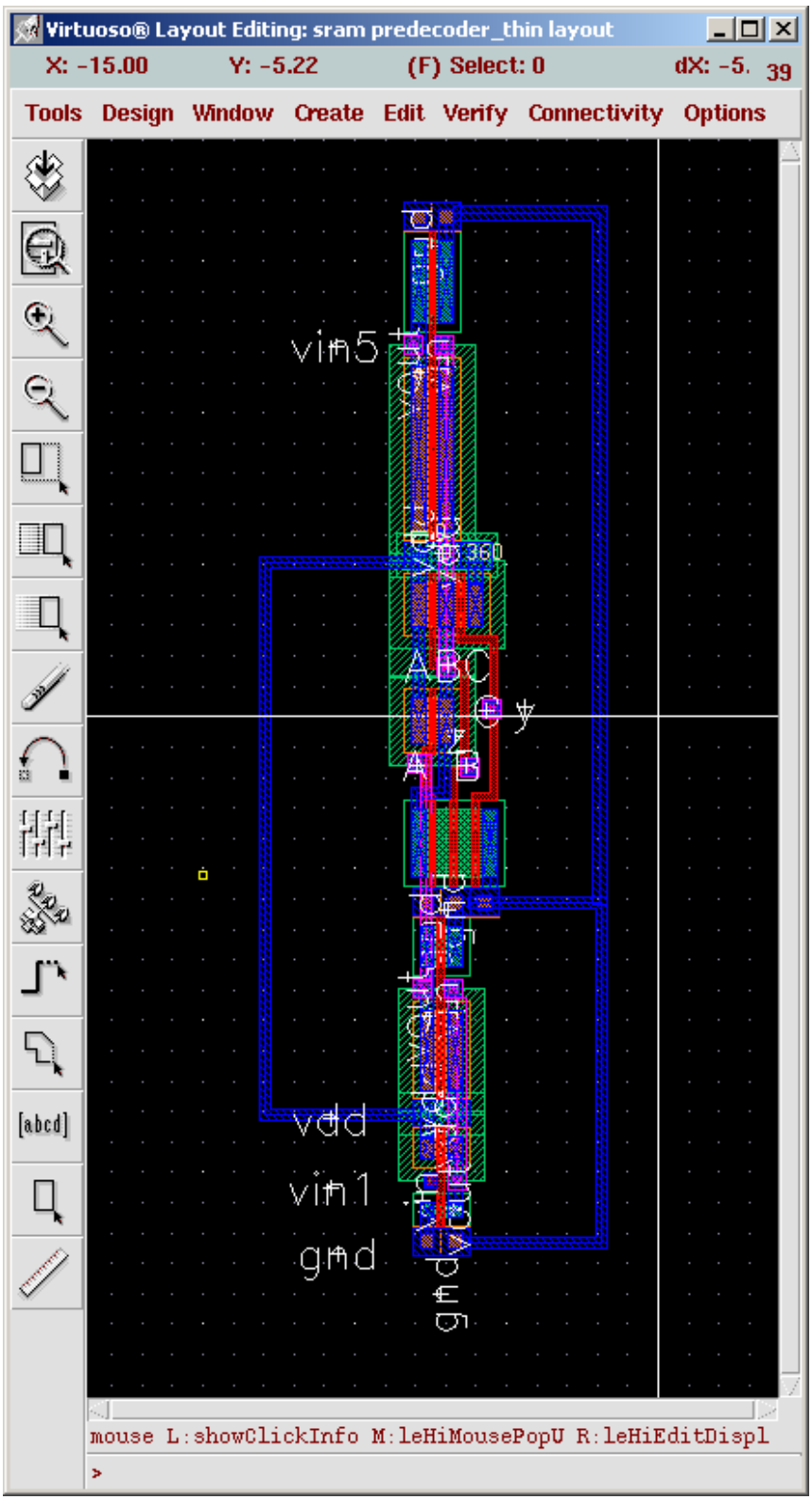
1	A
2	ABC
3	B
4	C
5	gnd
6	vdd

The net-lists match.

Schematic



Final Predecoder



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
11	nets
6	terminals
6	pmos
6	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

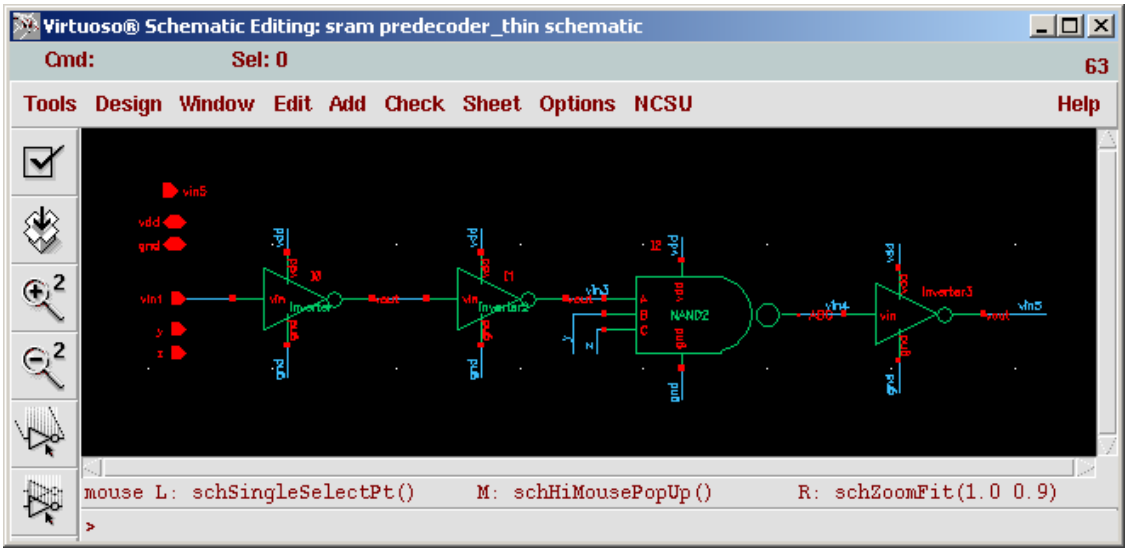
count	
11	nets
6	terminals
6	pmos
6	nmos

Terminal correspondence points

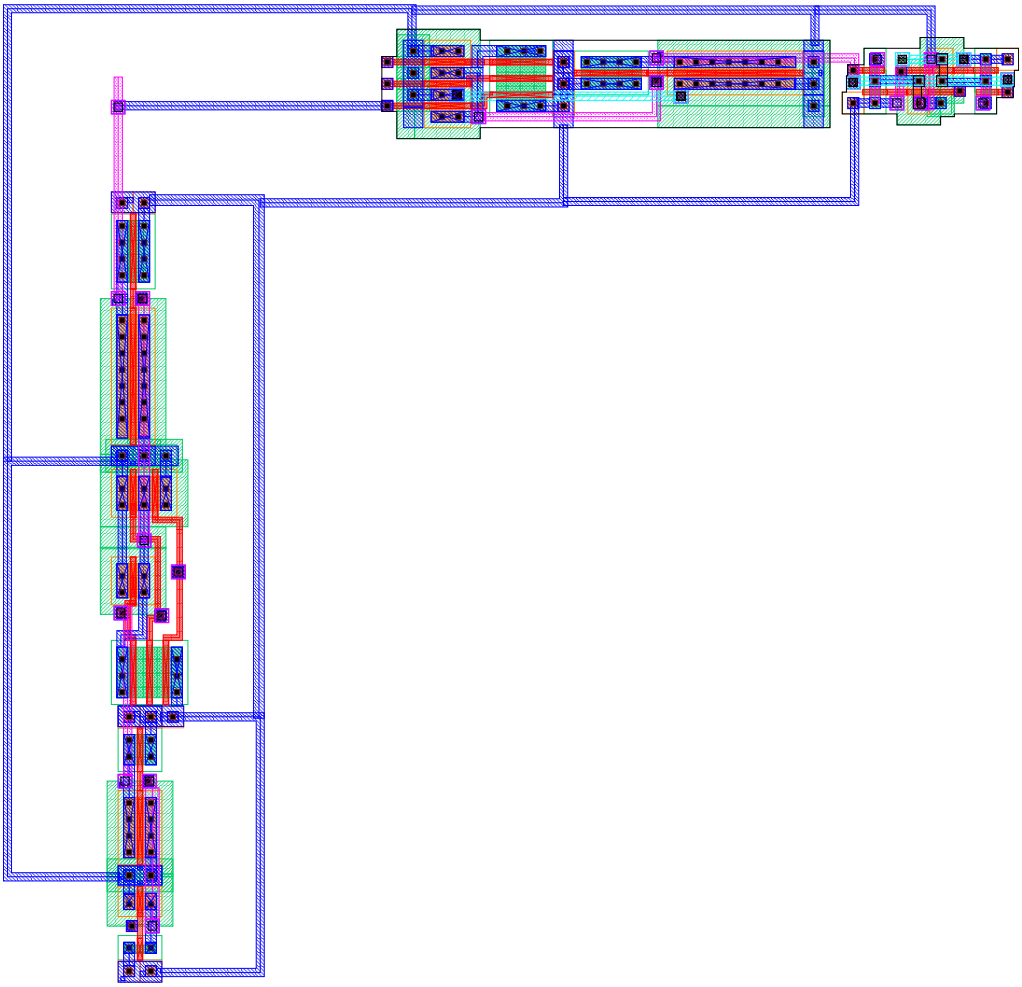
1	gnd
2	vdd
3	vin1
4	vin5
5	y
6	z

The net-lists match.

Schematic

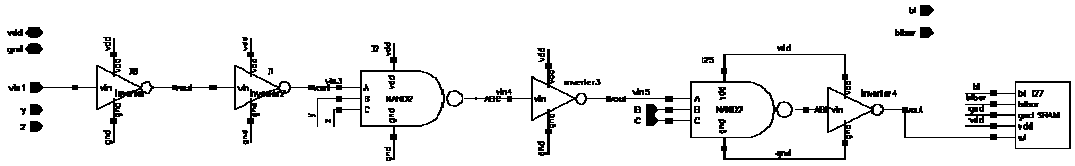


Predecoder+Postdecoder +SRAM



The metal 1 (blue) wires are gnd and vdd. These wires will be re-wired for final layout.

Schematic



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
21	nets
0	terminals
12	pmos
14	nmos

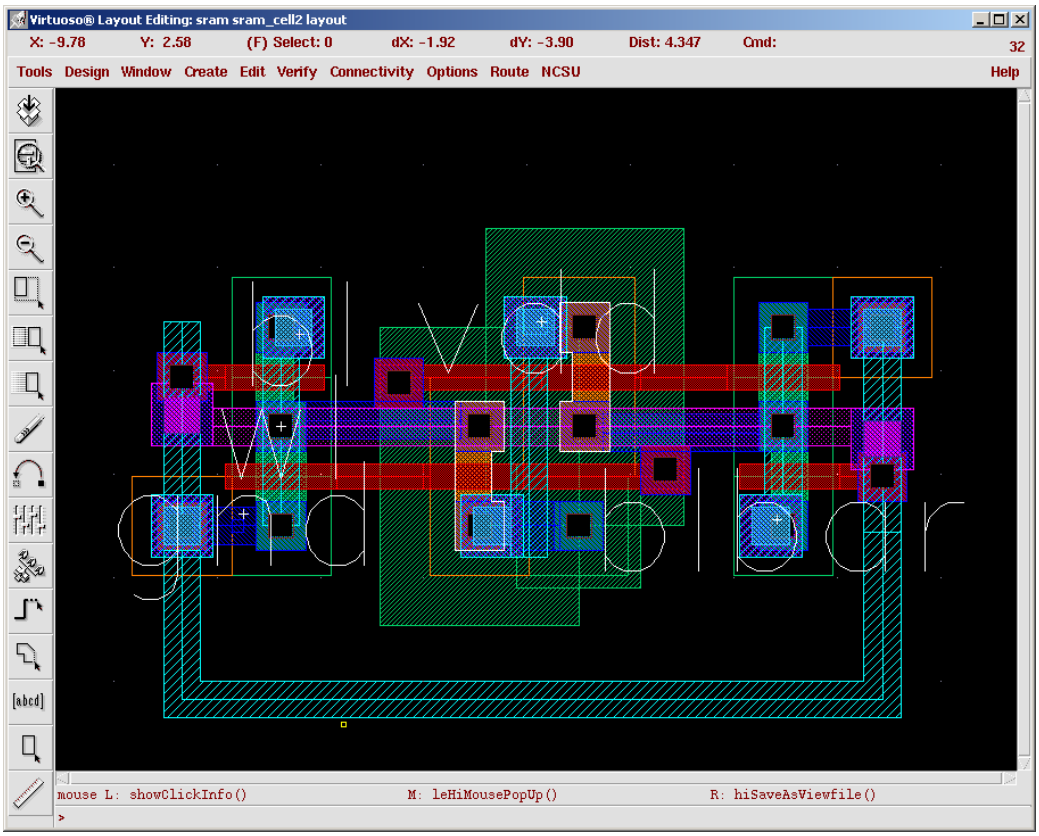
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
21	nets
9	terminals
12	pmos
14	nmos

4 net-list ambiguities were resolved by random selection.

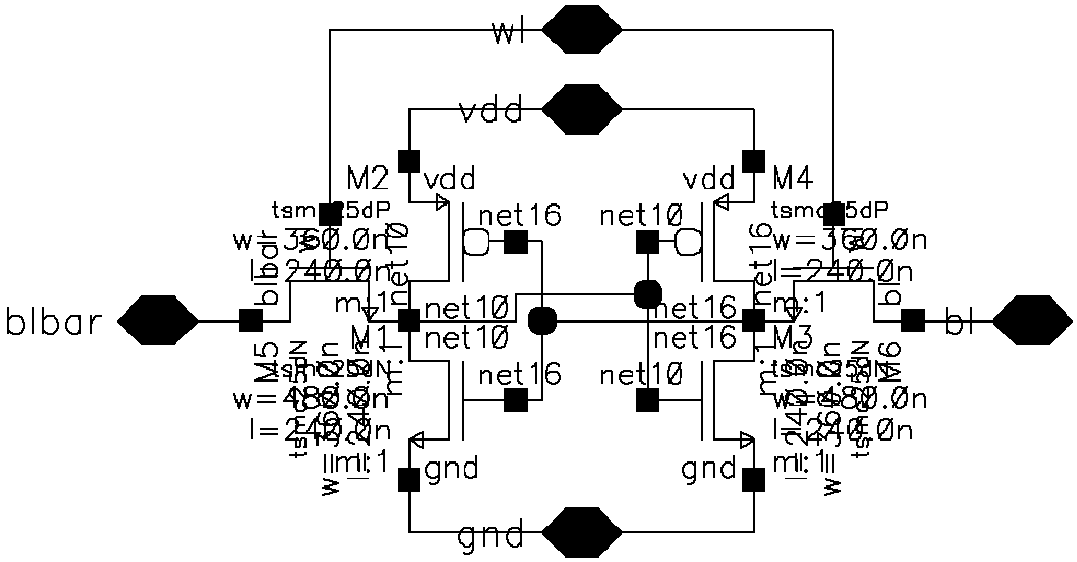
The net-lists match.

Rewiring SRAM Cell



Rewired the SRAM cell changing metal 2 to metal 3, metal 3 to metal 2.

Schematic



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
7	nets
5	terminals
2	pmos
4	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
7	nets
5	terminals
2	pmos
4	nmos

Terminal correspondence points

1	bl
2	blbar
3	gnd
4	vdd
5	wl

The net-lists match.

LVS Results (For Decoder with Re-wired SRAM Cell)

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
21	nets
0	terminals
12	pmos
14	nmos

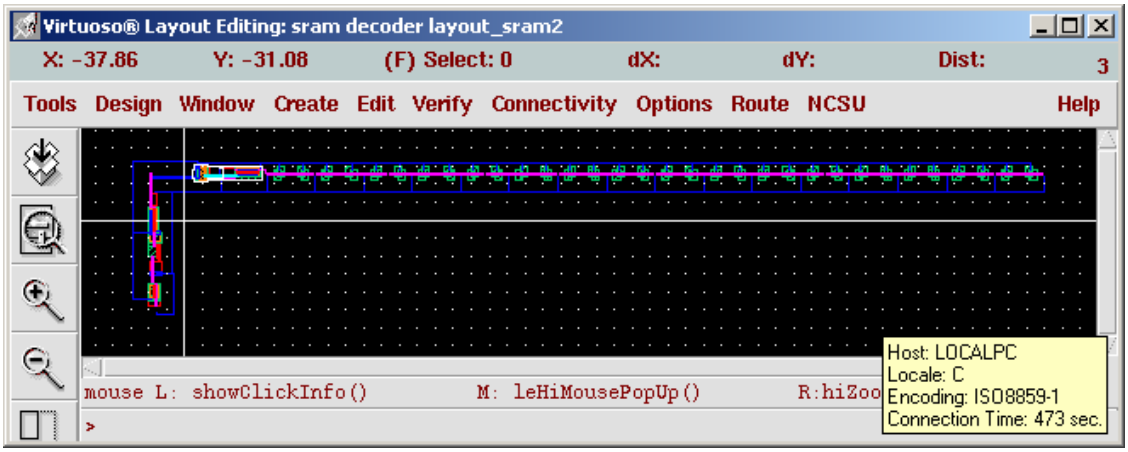
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
21	nets
9	terminals
12	pmos
14	nmos

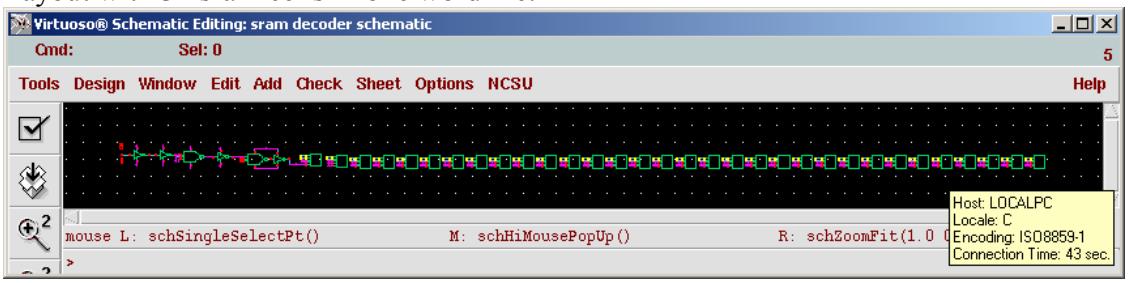
4 net-list ambiguities were resolved by random selection.

The net-lists match.

Predecoder+Postdecoder+Array of Re-wired SRAM Cells



Layout with 32 sram cells in one wordline.



Schematic with 32 sram cells

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
145	nets
0	terminals
74	pmos
138	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
145	nets
7	terminals
74	pmos
138	nmos

35 net-list ambiguities were resolved by random selection.

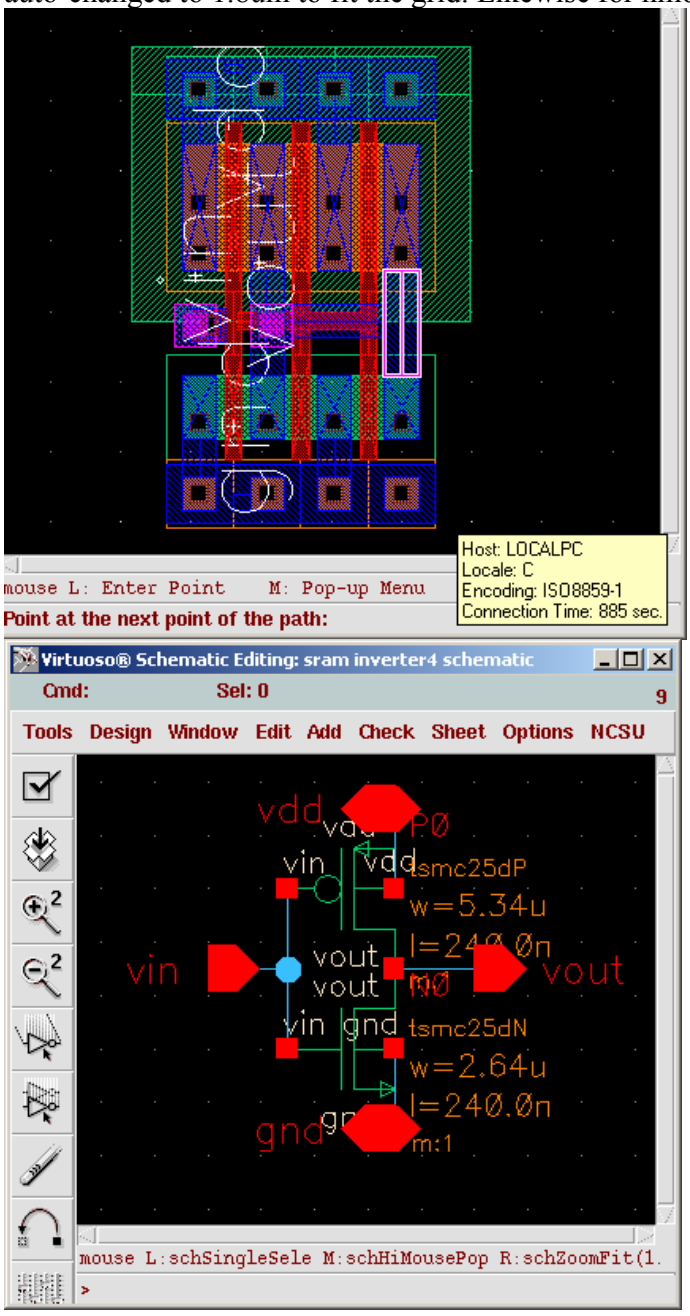
The net-lists match.

One Wordline HSPICE Extraction

one_wordline_final_extraction.sp

Minimizing Inverter 4

Changed multiplier of 1 to multiplier of 3. Width changed from 5.34um to 1.78um. Then auto-changed to 1.8um to fit the grid. Likewise for nmos.



pmos
5.34/3 = 1.78 -> 1.8um
nmos
2.64/3 = 0.88 -> 0.9um

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
3	pmos
3	nmos

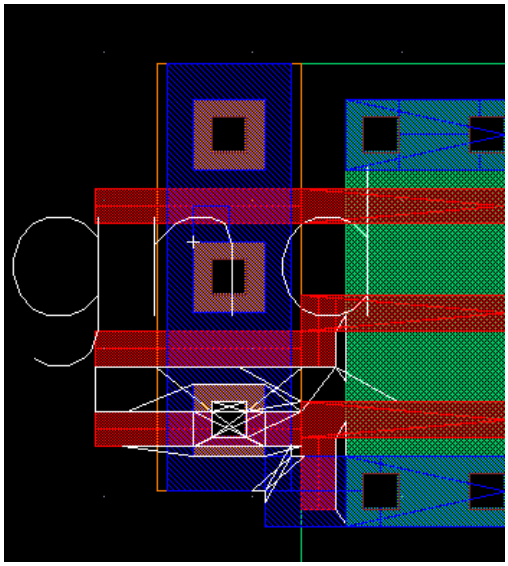
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Terminal correspondence points

1	gnd
2	vdd
3	vin
4	vout

The net-lists match.



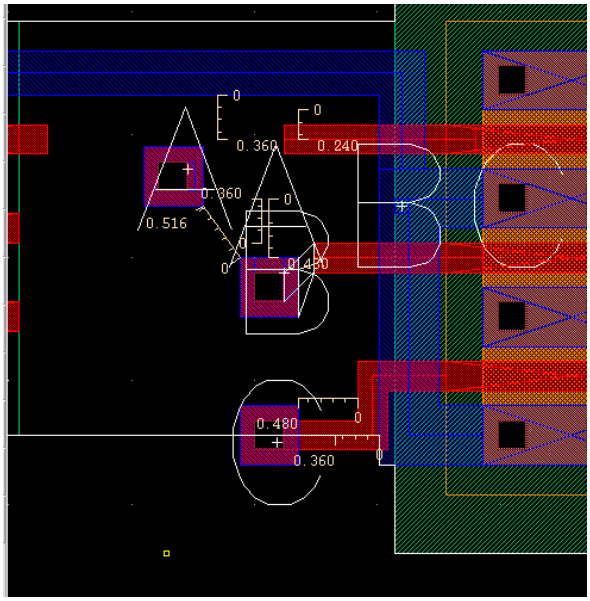
Minimizing Postdecoder NAND Gate

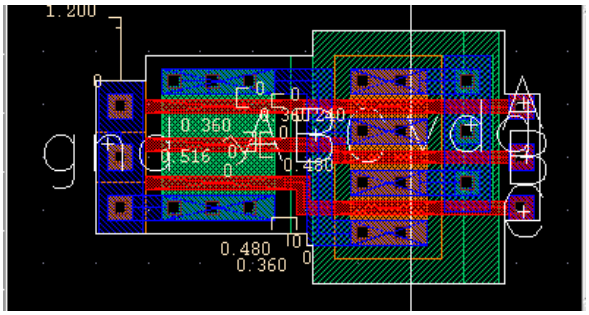
wanted to make the poly goes through the nmos instead of the pmos

But the poly are too close to the actives. So this doesn't work. (left, up)

Then I tried to put the contacts between pmos and nmos, but that makes the nand gate much longer. So this also doesn't work (left, down)

At the end, the original nand gate design was used. (right)





Minimzing the Whole Postdecoder

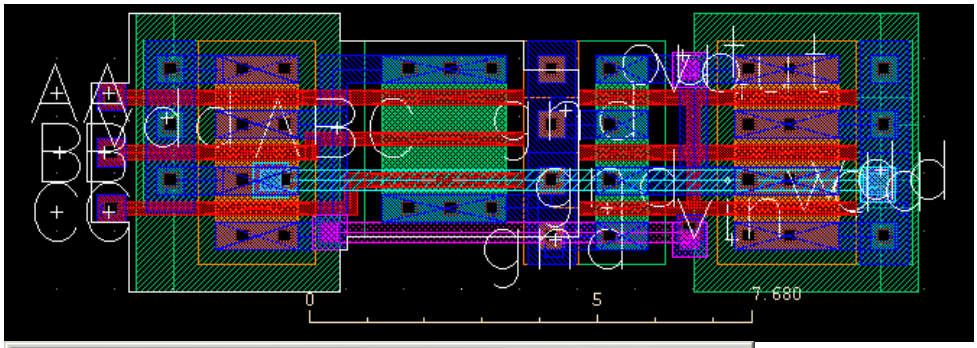
LVS Results

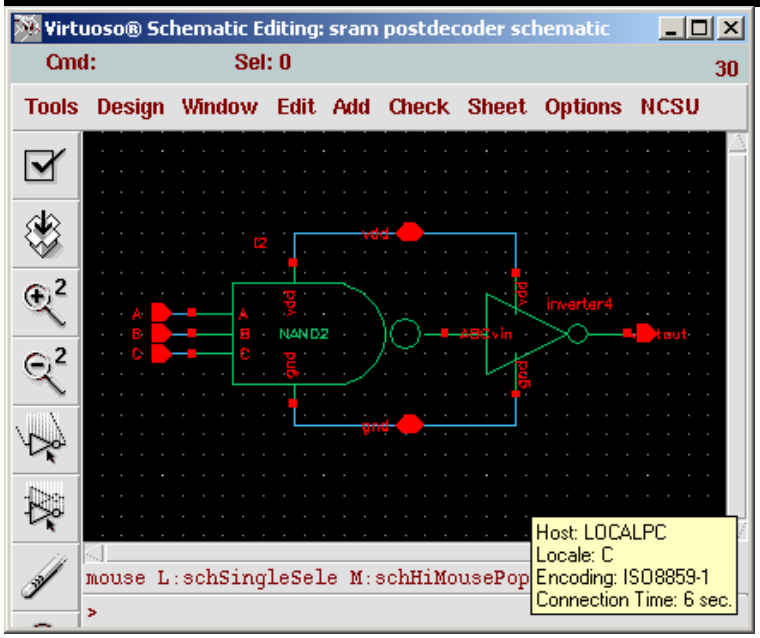
audit.out:
I /I0/P0
? Combined device: Transistor width mismatch: layout 5.40 um, schematic 5.34 um

I /I0/N0
? Combined device: Transistor width mismatch: layout 2.70 um, schematic 2.64 um

Because using 3 multipliers, there are round-offs of half a lambda. I solved this problem by changing the schematics of inverter 4.

Inverter 4 schematic changes
Pmos 5.34->5.40
Nmos 2.64-> 2.70





LVS Results Match

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
9	nets
6	terminals
6	pmos
6	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
9	nets
6	terminals
4	pmos
4	nmos

Terminal correspondence points

1	A
2	B
3	C
4	gnd
5	out
6	vdd

The net-lists match.

Minimzing the Inverter 3

Pmos 5.4-/2=2.7um ->2.7um
Nmos 2.7/2=1.35 -> 1.38um

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
2	pmos
2	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

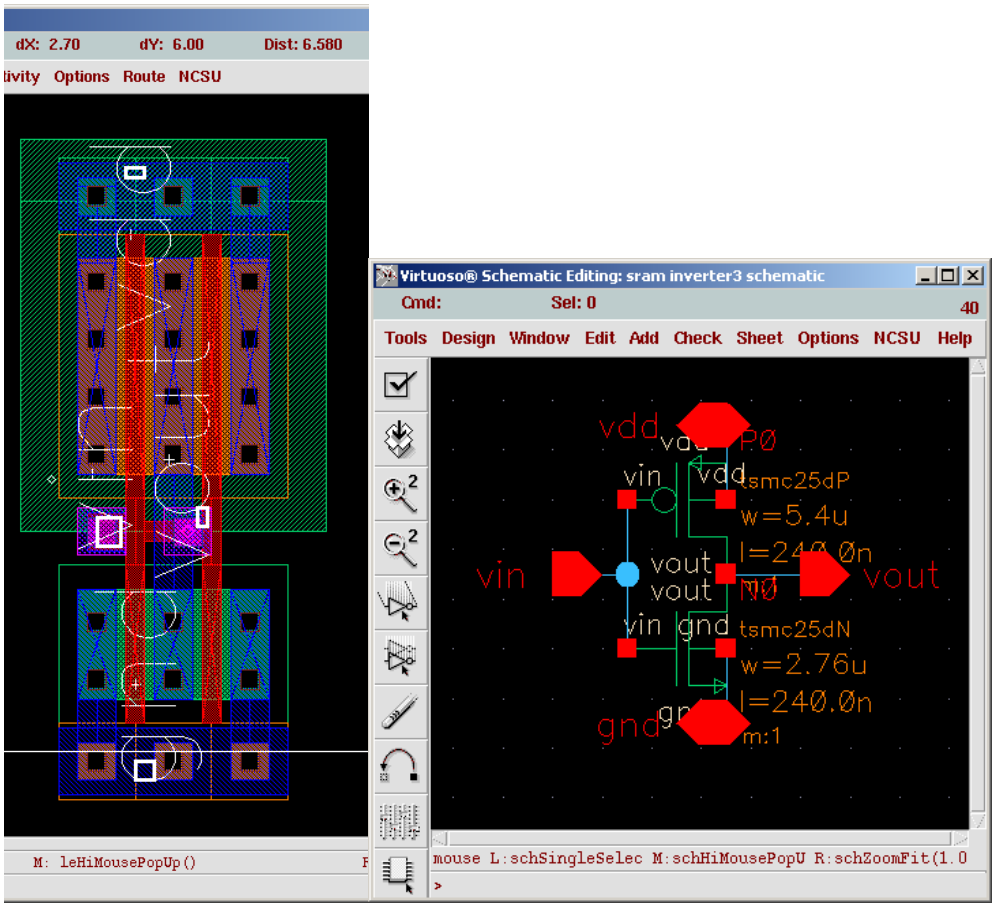
count	
4	nets
4	terminals
1	pmos
1	nmos

Terminal correspondence points

1	gnd
2	vdd
3	vin
4	vout

The net-lists match logically but have mismatched parameters.
I /N0
? Combined device: Transistor width mismatch: layout 2.76 um, schematic 2.70 um

Changing the schematic to solve this half a lambda problem.
Nmos 2.7->2.76um



LVS Results Match

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
2	pmos
2	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

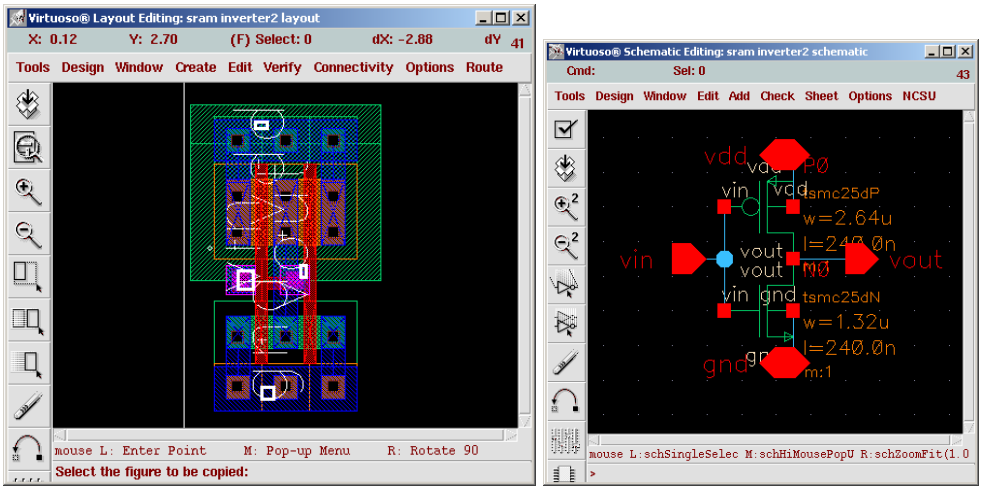
Terminal correspondence points

1	gnd
2	vdd
3	vin
4	vout

The net-lists match.

Minimzing the Inverter 2

Pmos 2.64/2=1.32um ->1.32um
Nmos 1.32/2=0.66 -> 0.66um



Schematic values were not changed.

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
4	nets
4	terminals
2	pmos
2	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

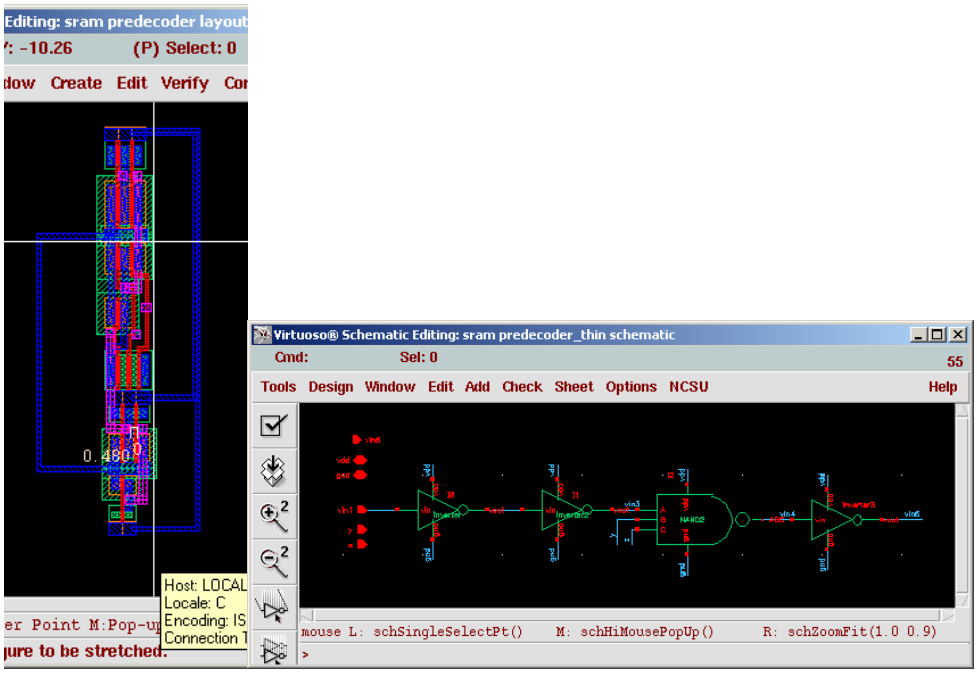
count	
4	nets
4	terminals
1	pmos
1	nmos

Terminal correspondence points

1	gnd
2	vdd
3	vin
4	vout

The net-lists match.

Minimizing the Whole Predecoder



LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
11	nets
6	terminals
8	pmos
8	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

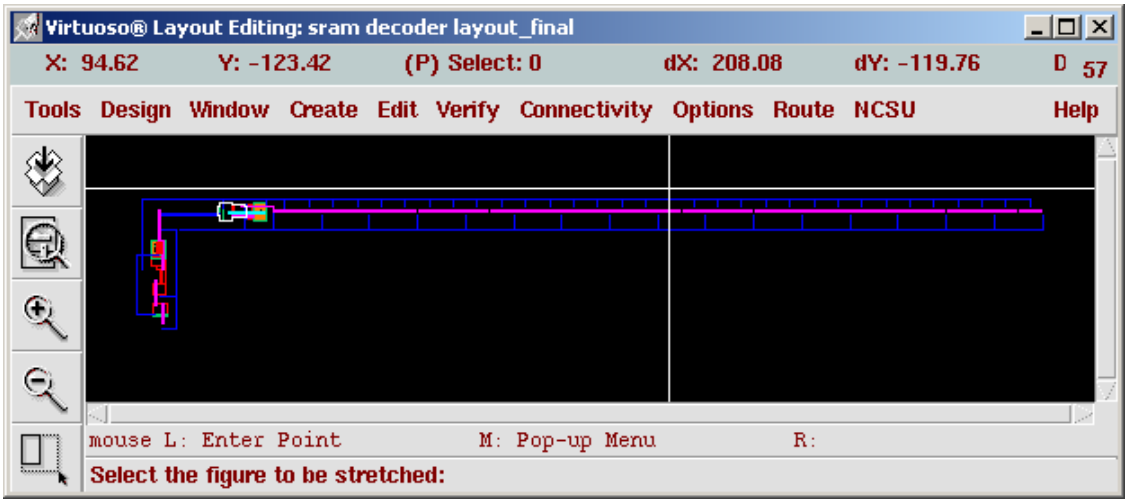
count	
11	nets
6	terminals
6	pmos
6	nmos

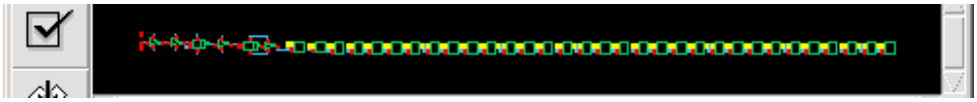
Terminal correspondence points

1	gnd
2	vdd
3	vin1
4	vin5
5	y
6	z

The net-lists match.

Minimizing Predecoder+Postdecoder+SRAM Array





LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
145	nets
0	terminals
78	pmos
142	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
145	nets
7	terminals
74	pmos
138	nmos

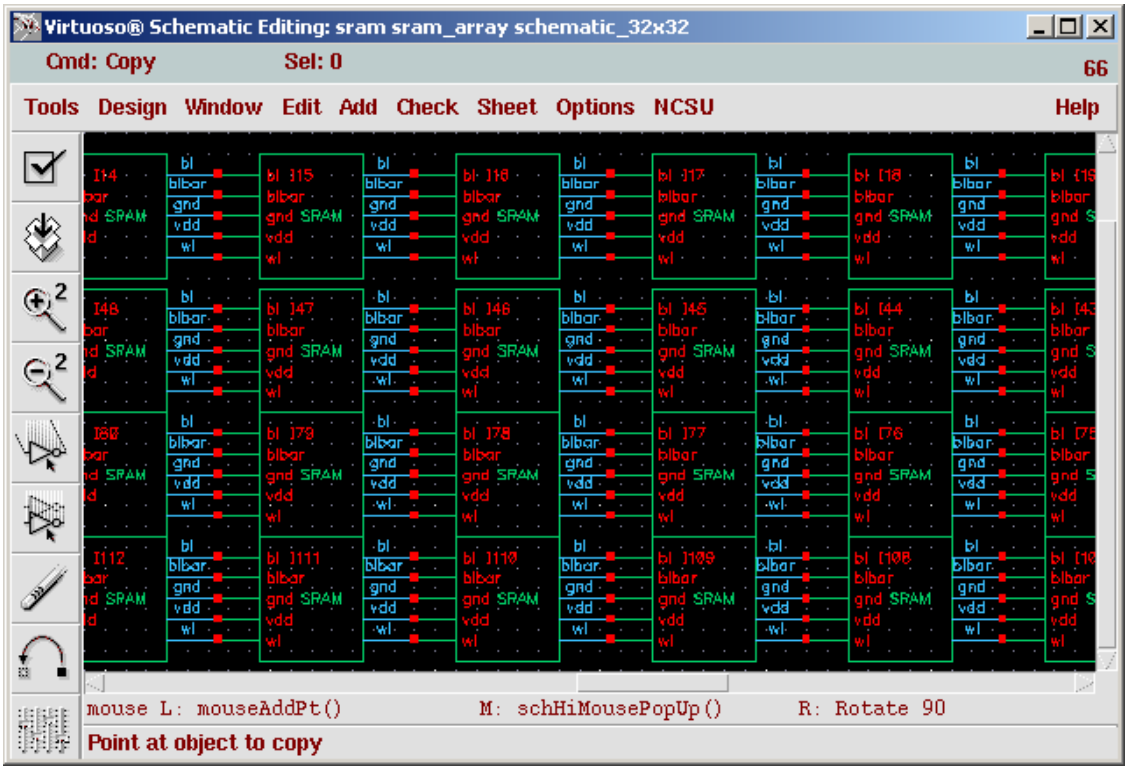
35 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic	
	instances		
un-matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	220	212	
total	220	212	
	nets		
un-matched	0	0	
merged	0	0	
pruned	0	0	
active	145	145	
total	145	145	
	terminals		
un-matched	0	0	
matched but different type	0	0	
total	0	7	

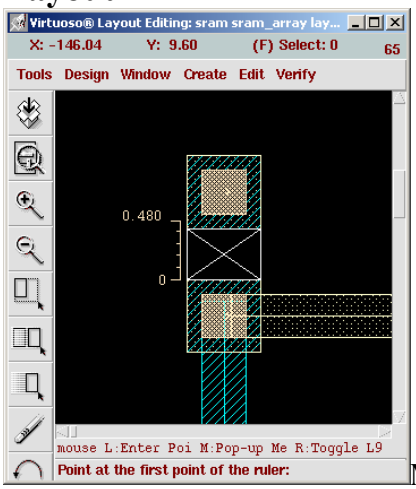
Array of SRAM Cells (4x32 SRAM Cells)

Schematics

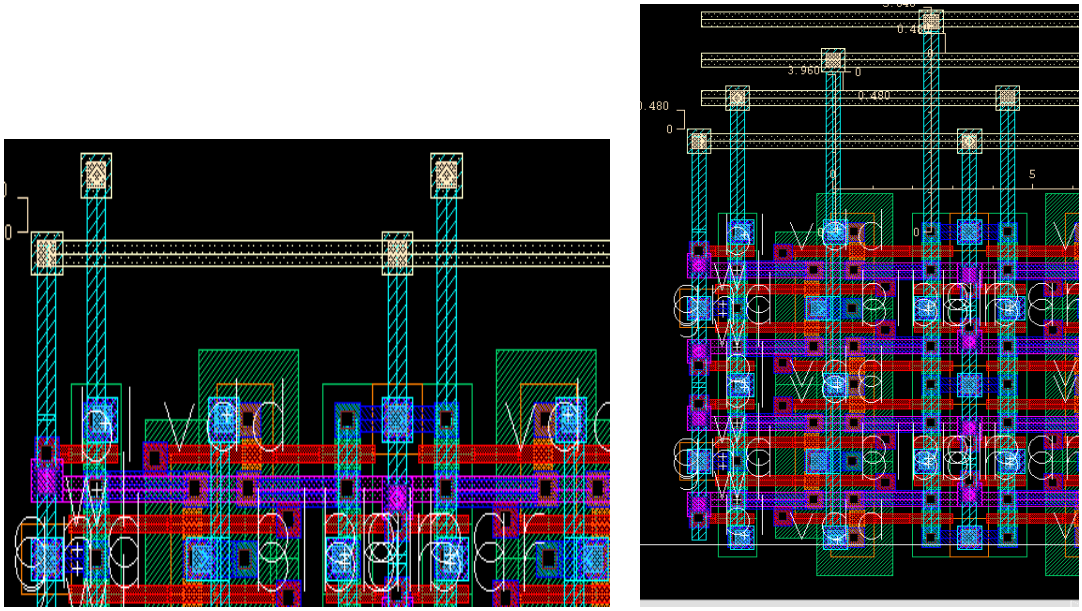


4 rows of 32 SRAM Cells Schematics.

Layout



Metal 4 spacing, 4 lambda.



(left) Connecting the gnd, bl, vdd, blbar through horizontal metal 4 layers.
(right) LVS passed 4x32 SRAM cells.

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
264	nets
0	terminals
256	pmos
512	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

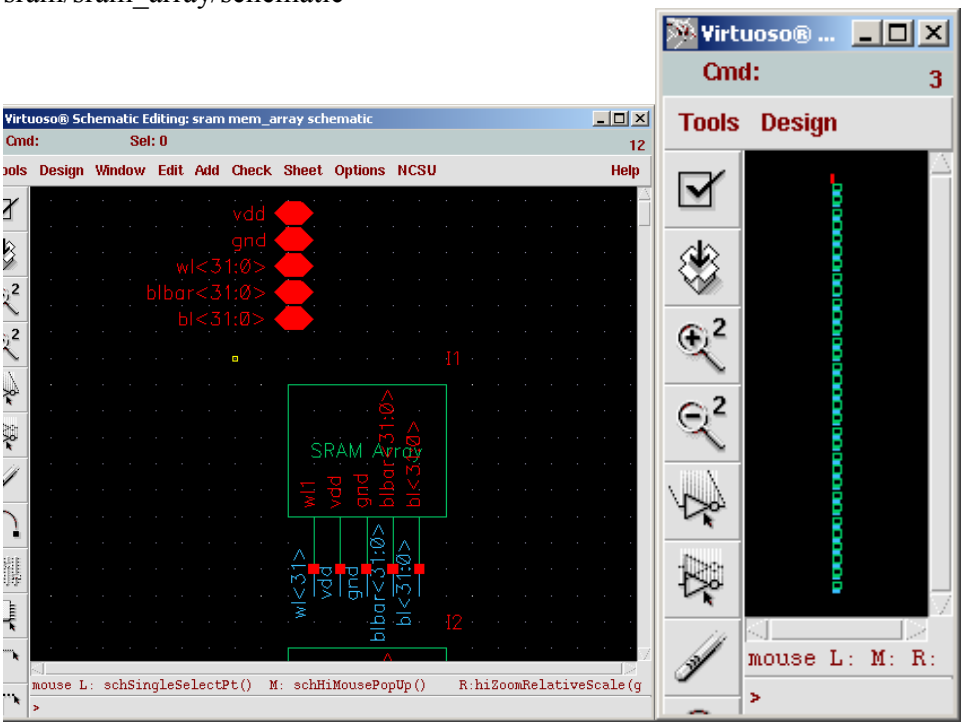
count	
264	nets
4	terminals
256	pmos
512	nmos

134 net-list ambiguities were resolved by random selection.

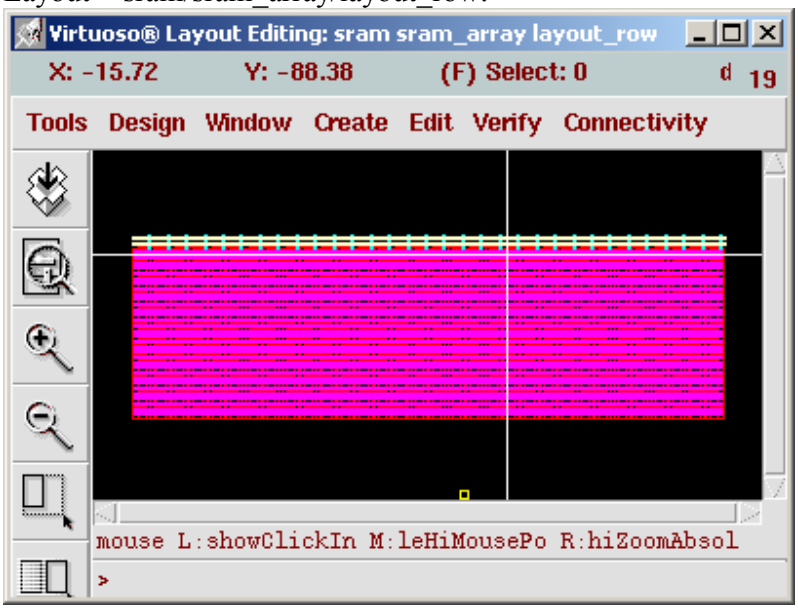
The net-lists match.

SRAM Array (32x32)

Schematic= sram/mem_array/schematic. Each symbol is an instantiation of sram/sram_array/schematic



Layout = sram/sram_array/layout_row.



DRC pass. Extract pass.

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
2146	nets
98	terminals
2048	pmos
4096	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
2146	nets
98	terminals
2048	pmos
4096	nmos

Terminal correspondence points

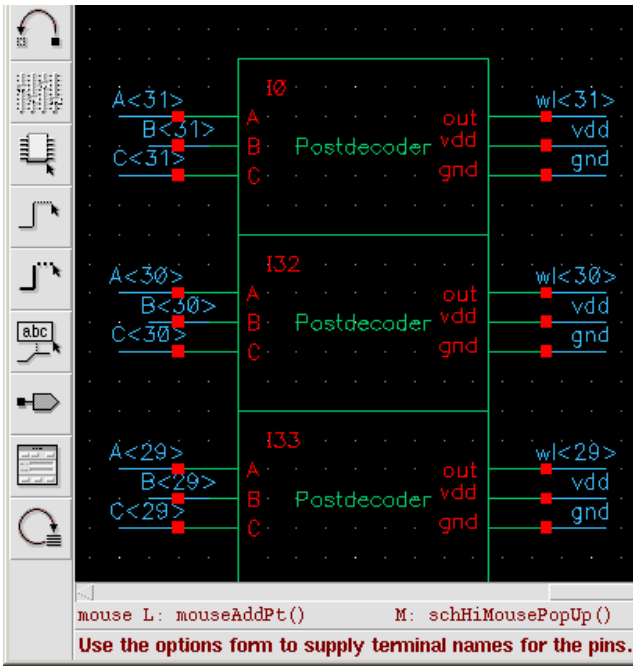
1	bl<0>
2	bl<10>
3	bl<11>
4	bl<12>
5	bl<13>
6	bl<14>
7	bl<15>
8	bl<16>
9	bl<17>
10	bl<18>
11	bl<19>
12	bl<1>
13	bl<20>
14	bl<21>
15	bl<22>
16	bl<23>
17	bl<24>
18	bl<25>
19	bl<26>
20	bl<27>
21	bl<28>
22	bl<29>
23	bl<2>
24	bl<30>
25	bl<31>
26	bl<3>
27	bl<4>
28	bl<5>
29	bl<6>
30	bl<7>
31	bl<8>
32	bl<9>
33	blbar<0>
34	blbar<10>

35 blbar<11>
36 blbar<12>
37 blbar<13>
38 blbar<14>
39 blbar<15>
40 blbar<16>
41 blbar<17>
42 blbar<18>
43 blbar<19>
44 blbar<1>
45 blbar<20>
46 blbar<21>
47 blbar<22>
48 blbar<23>
49 blbar<24>
50 blbar<25>
51 blbar<26>
52 blbar<27>
53 blbar<28>
54 blbar<29>
55 blbar<2>
56 blbar<30>
57 blbar<31>
58 blbar<3>
59 blbar<4>
60 blbar<5>
61 blbar<6>
62 blbar<7>
63 blbar<8>
64 blbar<9>
65 gnd
66 vdd
67 wl<0>
68 wl<10>
69 wl<11>
70 wl<12>
71 wl<13>
72 wl<14>
73 wl<15>
74 wl<16>
75 wl<17>
76 wl<18>
77 wl<19>
78 wl<1>
79 wl<20>
80 wl<21>
81 wl<22>
82 wl<23>
83 wl<24>
84 wl<25>
85 wl<26>
86 wl<27>
87 wl<28>
88 wl<29>
89 wl<2>

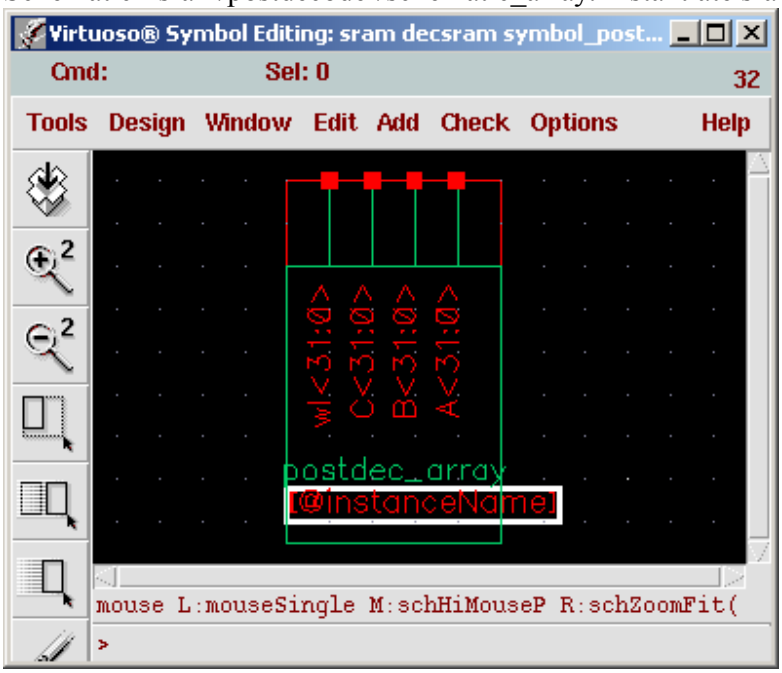
90	wl<30>
91	wl<31>
92	wl<3>
93	wl<4>
94	wl<5>
95	wl<6>
96	wl<7>
97	wl<8>
98	wl<9>

The net-lists match.

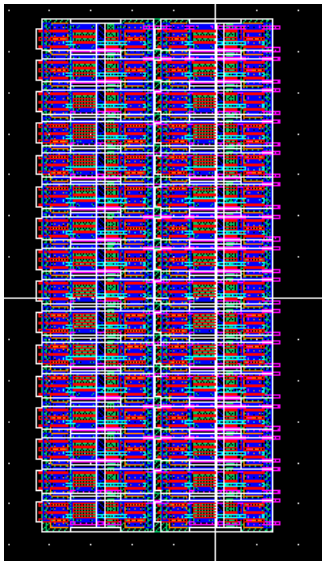
Post Decoder Array (32 Instants)



Schematic= sram/postdecoder/schematic_array. Instantiate sram/postdecoder/symbol.



Symbol=Sram/postdecoder/symbol_array



Layout=sram/postdecoder/layout_array

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
226	nets
0	terminals
192	pmos
192	nmos

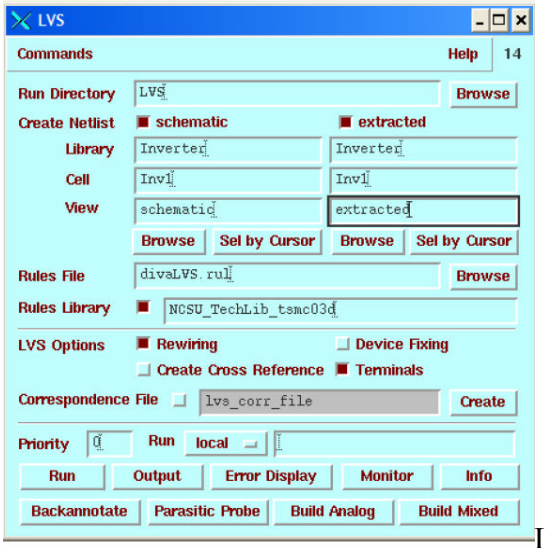
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
226	nets
128	terminals
128	pmos
128	nmos

96 net-list ambiguities were resolved by random selection.

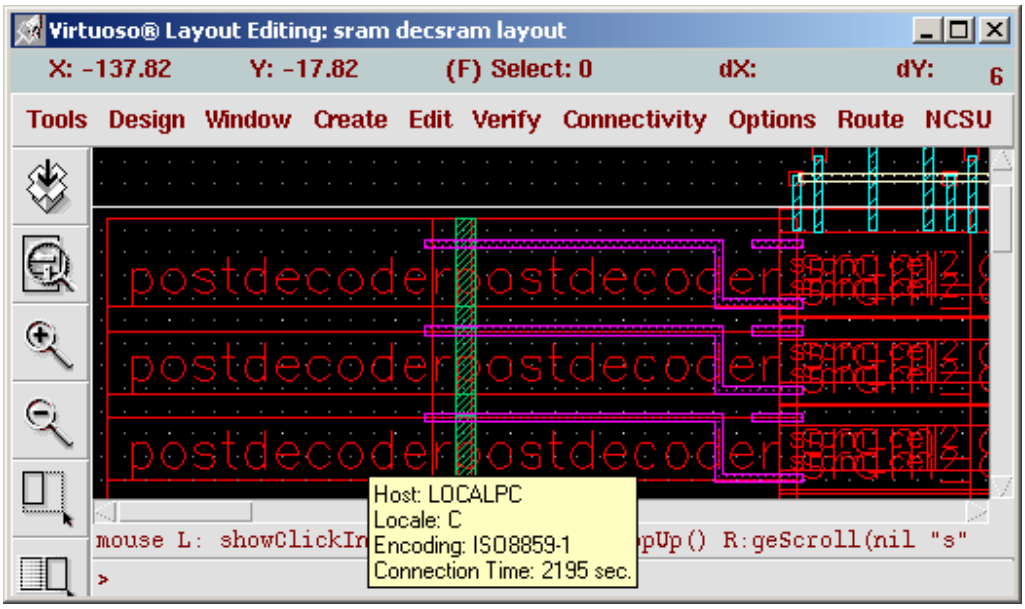
The net-lists match.

LVS Window Screen from Labs



LVS from the lab

32x32 SRAM Cells + 32-Postdecoder Array



Layout = sram/dec_sram/layout

LVS mysteriously doesn't even generate the report. Let's go back to the postdecoder array and do LVS on that first. (later) the postdecoder array works. But still got this error.

Found the error… I thought
WARNING dbSave: Failed to save cellView (decsram extracted). Disc quota exceeded

The error was never found. After 2 hours of finding why LVS failed. I gave up and drew the cell from scrach again. Then I passed LVS.

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
2146	nets
98	terminals
2048	pmos
4096	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
2146	nets
98	terminals
2048	pmos
4096	nmos

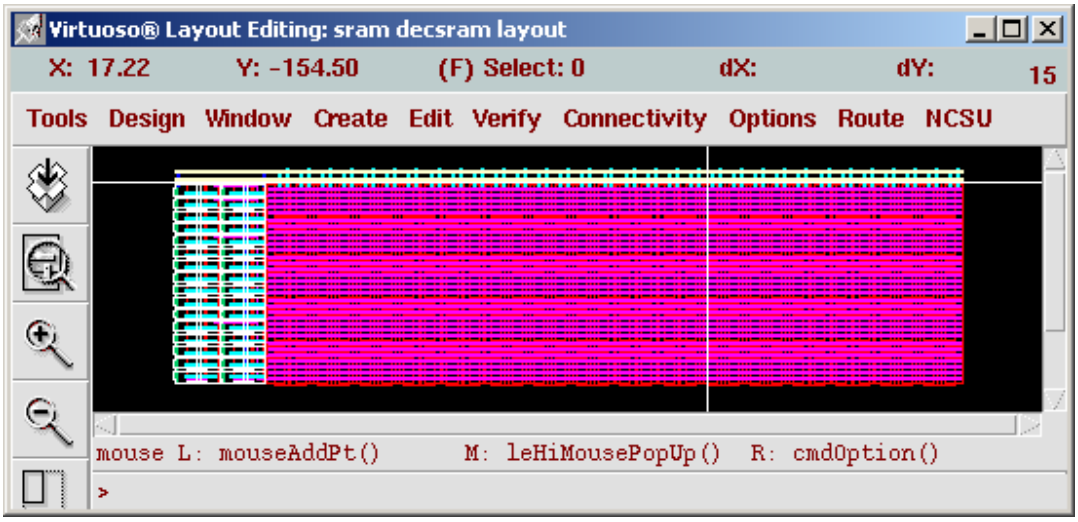
Terminal correspondence points

1	bl<0>
2	bl<10>
3	bl<11>
4	bl<12>
5	bl<13>
6	bl<14>
7	bl<15>
8	bl<16>
9	bl<17>
10	bl<18>
11	bl<19>
12	bl<1>
13	bl<20>
14	bl<21>
15	bl<22>
16	bl<23>
17	bl<24>
18	bl<25>
19	bl<26>
20	bl<27>
21	bl<28>
22	bl<29>
23	bl<2>
24	bl<30>
25	bl<31>
26	bl<3>
27	bl<4>
28	bl<5>
29	bl<6>
30	bl<7>

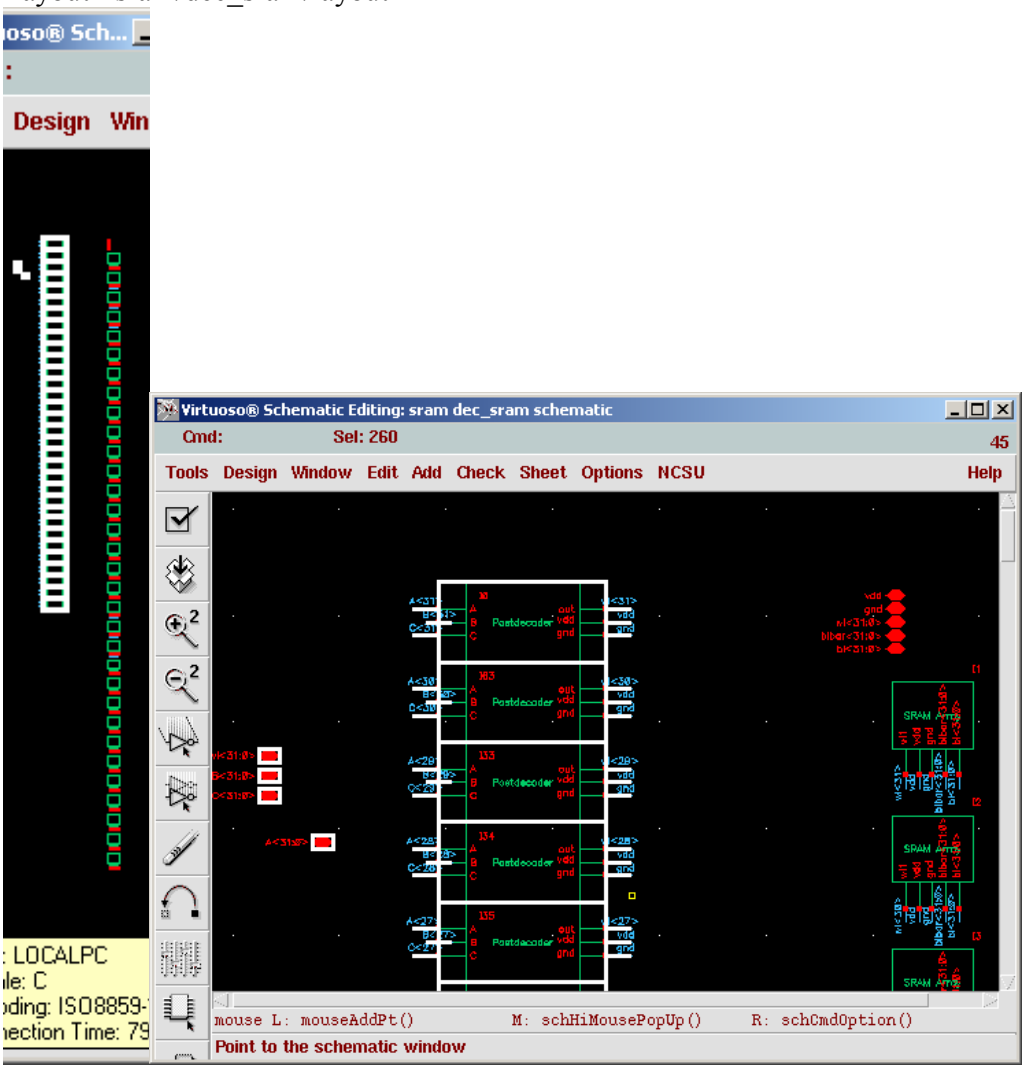
31 bl<8>
32 bl<9>
33 blbar<0>
34 blbar<10>
35 blbar<11>
36 blbar<12>
37 blbar<13>
38 blbar<14>
39 blbar<15>
40 blbar<16>
41 blbar<17>
42 blbar<18>
43 blbar<19>
44 blbar<1>
45 blbar<20>
46 blbar<21>
47 blbar<22>
48 blbar<23>
49 blbar<24>
50 blbar<25>
51 blbar<26>
52 blbar<27>
53 blbar<28>
54 blbar<29>
55 blbar<2>
56 blbar<30>
57 blbar<31>
58 blbar<3>
59 blbar<4>
60 blbar<5>
61 blbar<6>
62 blbar<7>
63 blbar<8>
64 blbar<9>
65 gnd
66 vdd
67 wl<0>
68 wl<10>
69 wl<11>
70 wl<12>
71 wl<13>
72 wl<14>
73 wl<15>
74 wl<16>
75 wl<17>
76 wl<18>
77 wl<19>
78 wl<1>
79 wl<20>
80 wl<21>
81 wl<22>
82 wl<23>
83 wl<24>
84 wl<25>
85 wl<26>

86 wl<27>
87 wl<28>
88 wl<29>
89 wl<2>
90 wl<30>
91 wl<31>
92 wl<3>
93 wl<4>
94 wl<5>
95 wl<6>
96 wl<7>
97 wl<8>
98 wl<9>

The net-lists match.

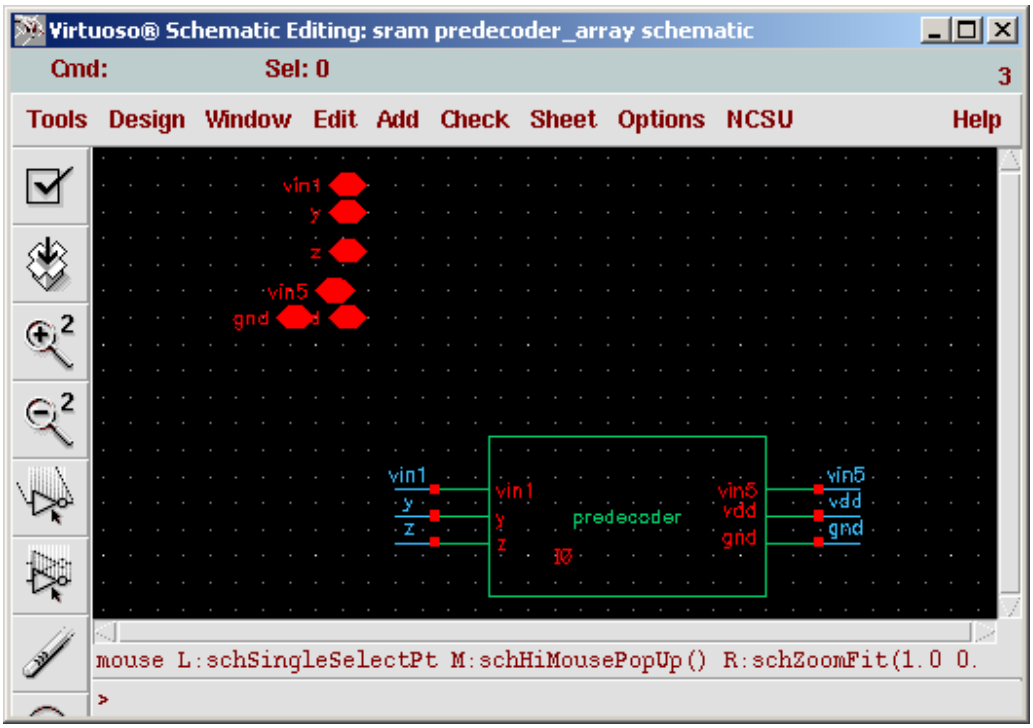


Layout= sram/dec_sram/layout

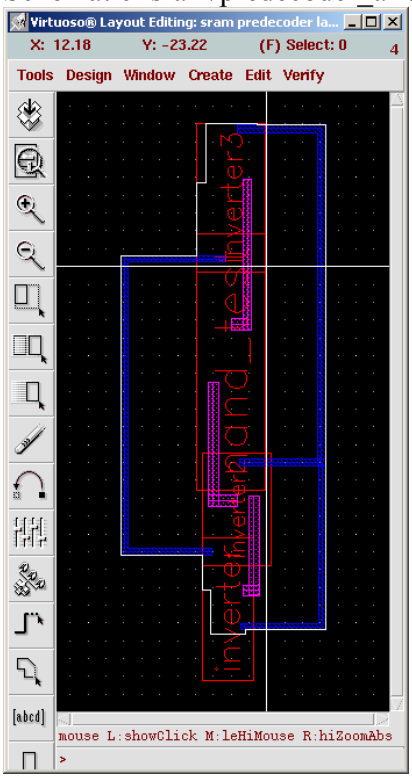


Schematic=sram/sram_dec/schematic

Predecoder Symbol



Schematic=sram/predecoder_array/schematic



Layout=sram/predecoder/layout_final

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
11	nets
6	terminals
8	pmos
8	nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

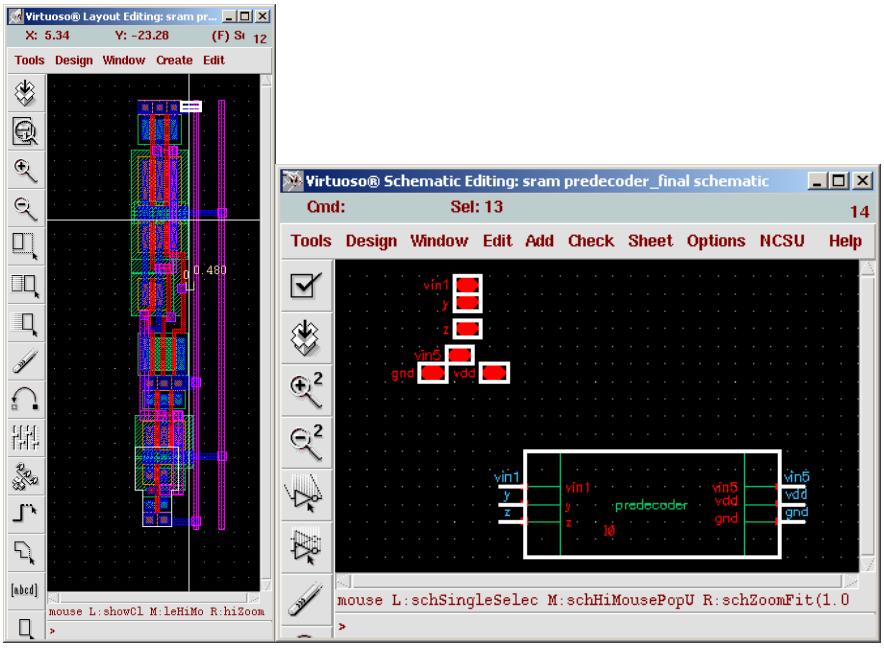
count	
11	nets
6	terminals
6	pmos
6	nmos

Terminal correspondence points

1	gnd
2	vdd
3	vin1
4	vin5
5	y
6	z

The net-lists match.

Predecoder Final



Layout=sram/precoder_final/layout, schematic= sram/precoder_final/schematic

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
131	nets
0	terminals
64	pmos
128	nmos

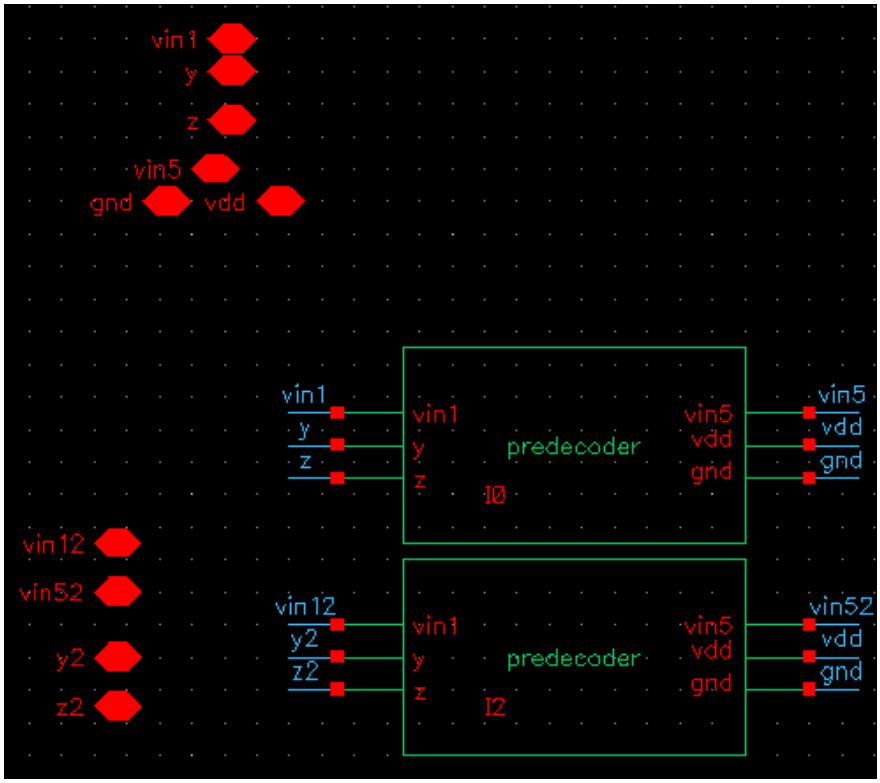
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
131	nets
67	terminals
64	pmos
128	nmos

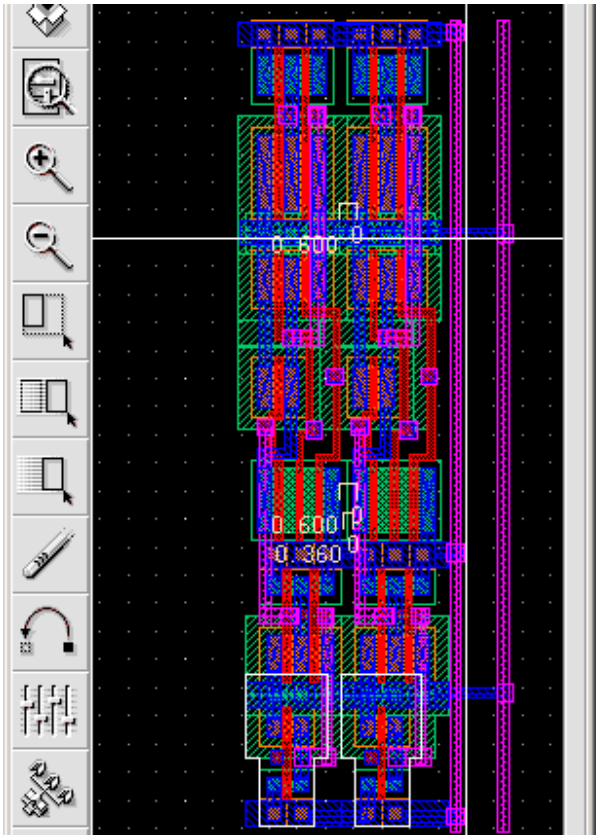
33 net-list ambiguities were resolved by random selection.

The net-lists match.

2 Predecoder



Schematic=sram/predecoder_array/schematic



Layout=sram/predecoder_array/layout

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
20	nets
0	terminals
16	pmos
16	nmos

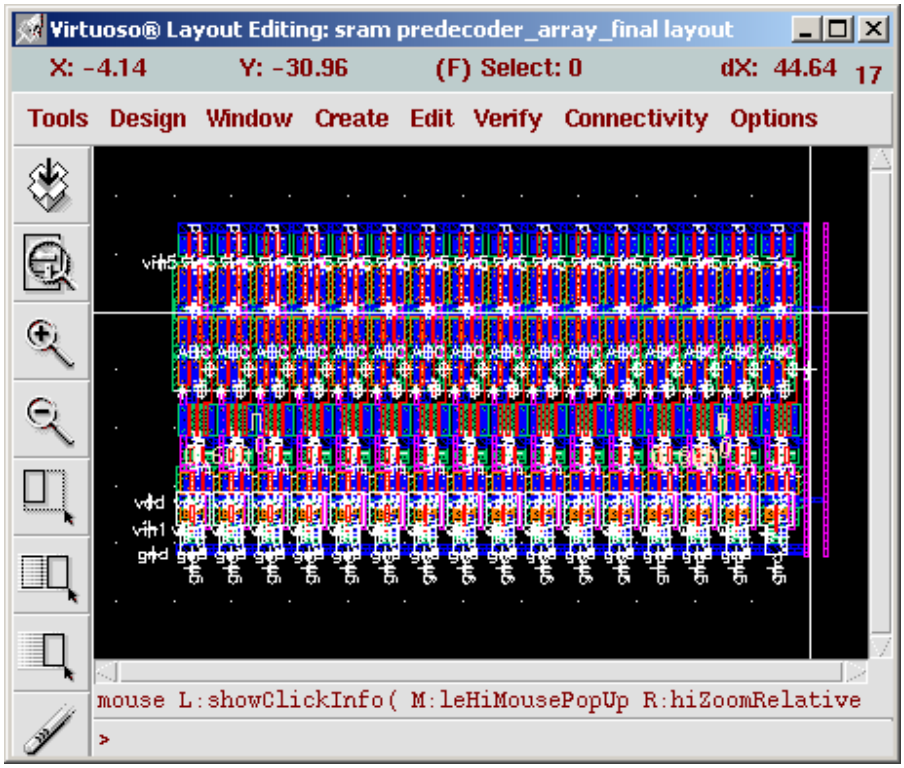
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
20	nets
10	terminals
12	pmos
12	nmos

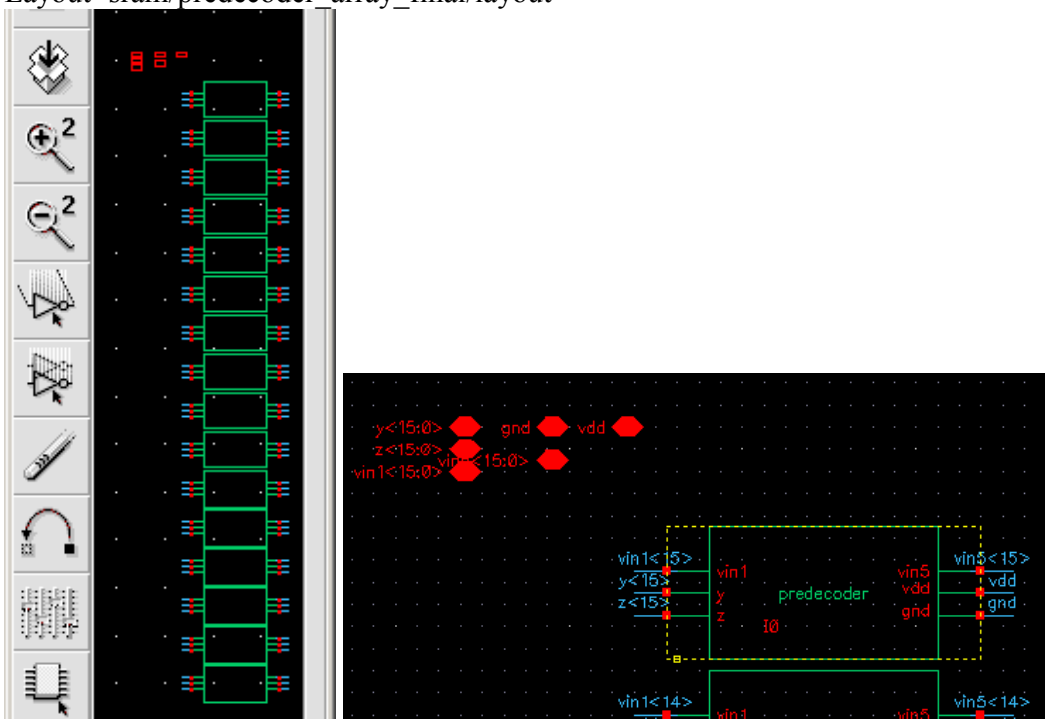
4 net-list ambiguities were resolved by random selection.

The net-lists match.

Predecoder Array (16 Instants)



Layout=sram/predecoder_array_final/layout



Schematic=sram/predecoder_array_final/schematic

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
146	nets
0	terminals
128	pmos
128	nmos

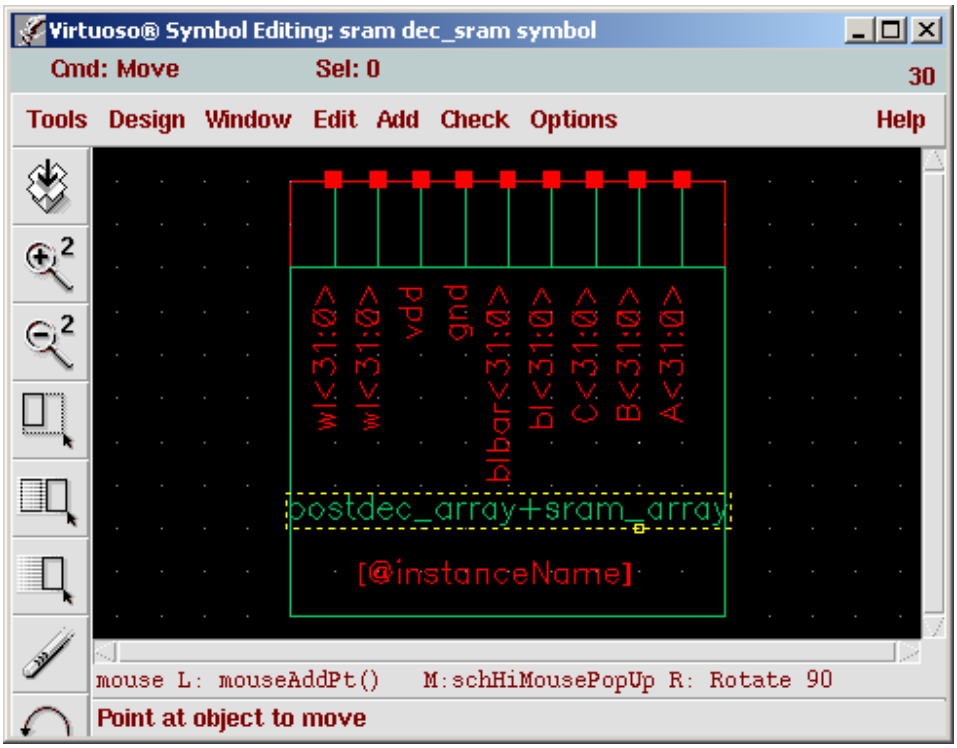
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
146	nets
66	terminals
96	pmos
96	nmos

32 net-list ambiguities were resolved by random selection.

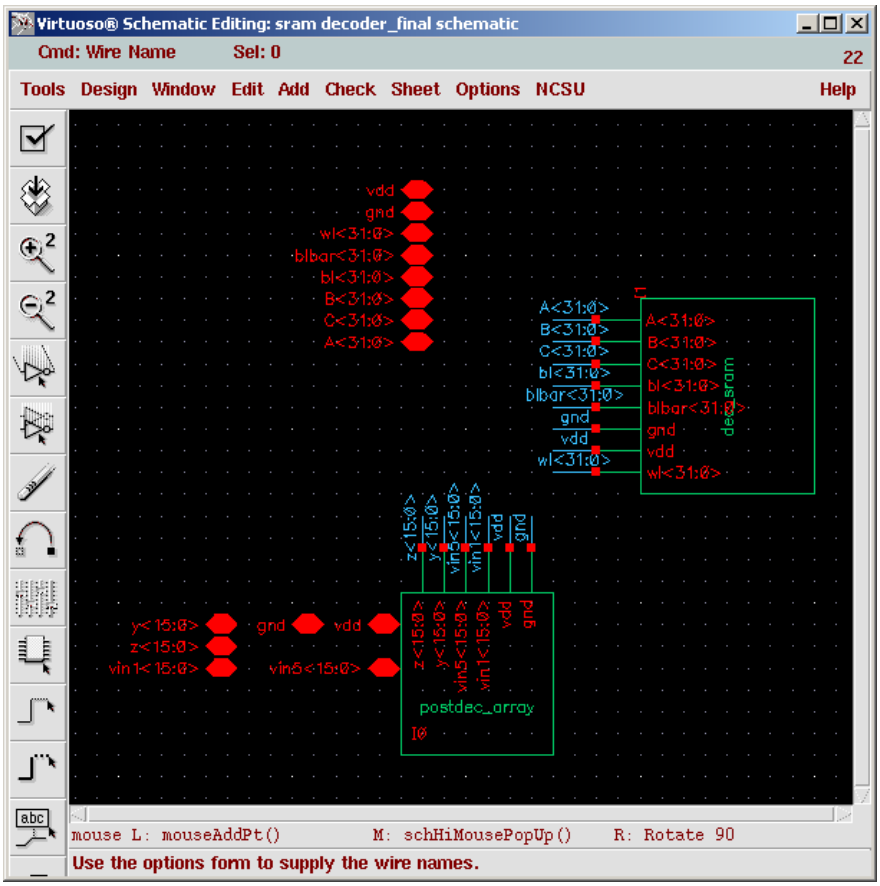
The net-lists match.

16-Predecoder + 32-Postdecoder + 32x32-SRAM

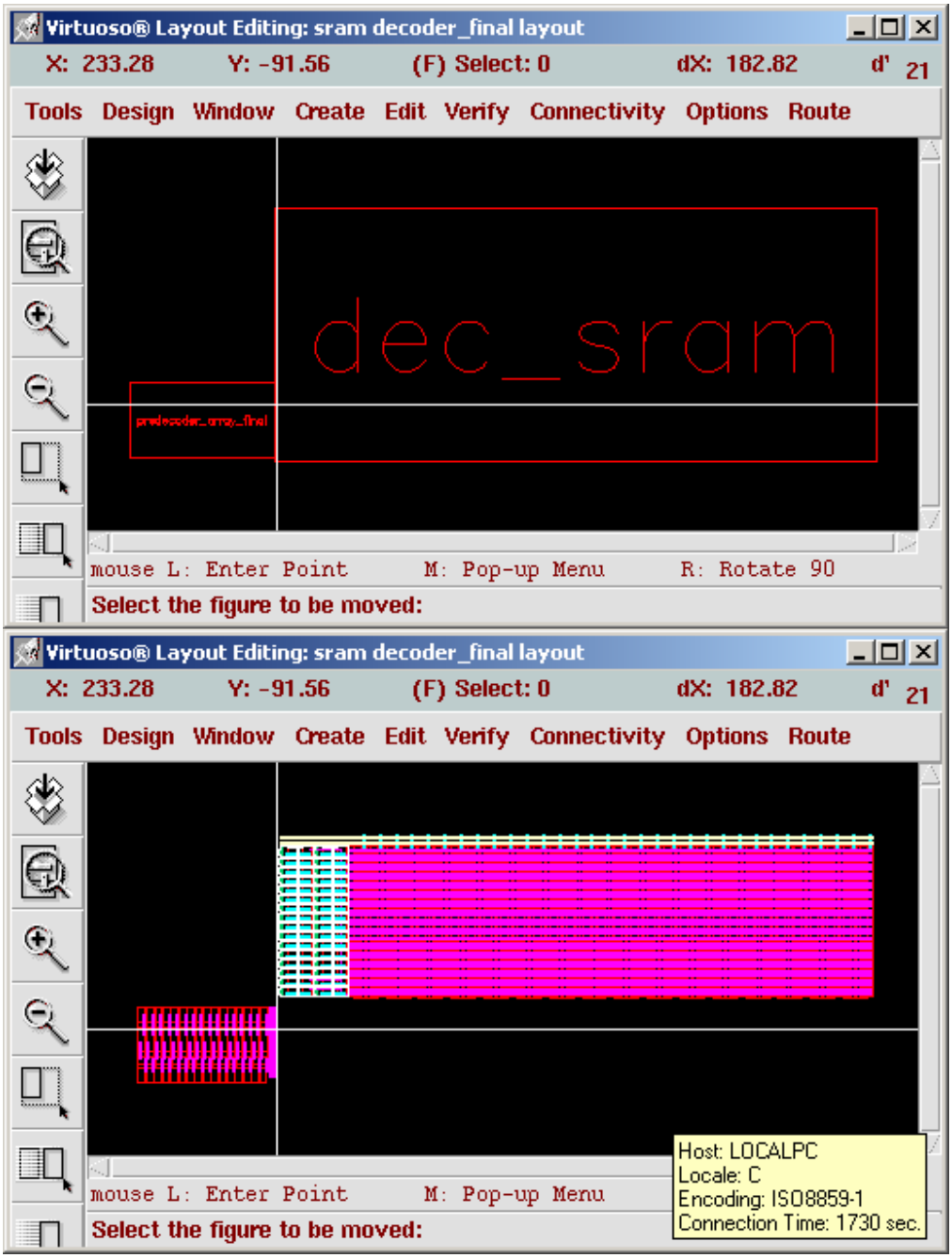


Symbol = sram/dec_sram/symbol

Symbol=sram/predecoder_array_final/symbol



Schematic=sram/decoder_final/schematic



Layout=sram/decoder_final/layout

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
2482	nets
0	terminals
2368	pmos
4416	nmos

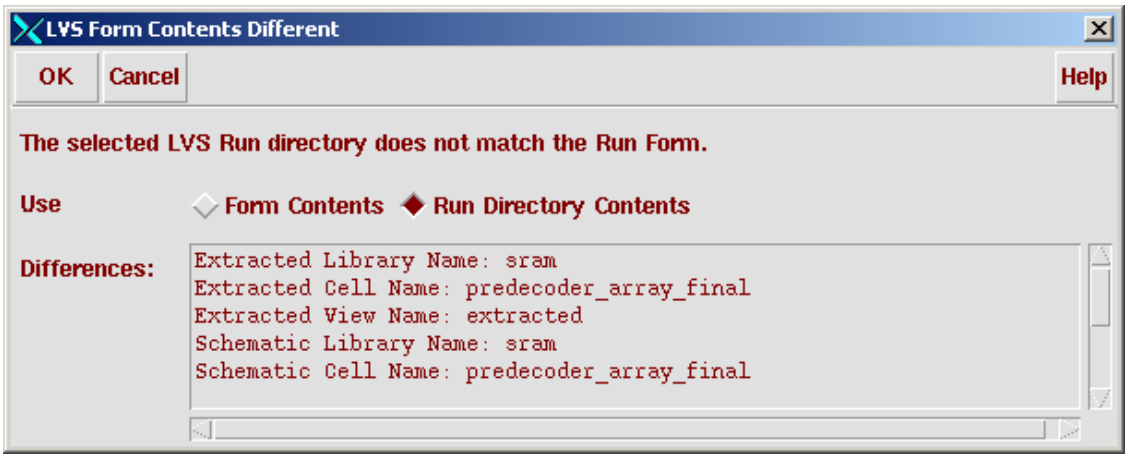
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
2482	nets
258	terminals
2272	pmos
4320	nmos

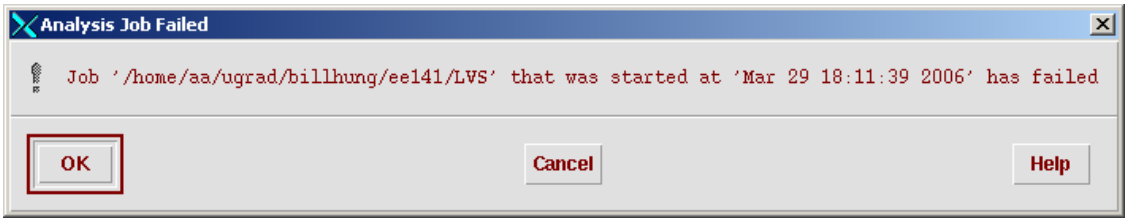
161 net-list ambiguities were resolved by random selection.

The net-lists match.

LVS (mysteriously) Failed



"OK"



Our group has had this LVS-failed problem for hours. We have re-done the procedure again and again, checked the lab procedures, but nothing could get rid of the LVS-failed problem. We made sure the account has plenty of quota. We are also sure we didn't delete any cadence files. We restarted Cadence, restarted the SSH, and we tried to login to cory and quasar to solve this

problem.

Suddenly all the cells that passed LVS before start giving us the
LVS -failed message: "Job '/home/aa/ugrad/billhung/ee141/LVS' that was
started at 'Mar 29 17:36:19 2006' has failed"
None of the cells succeeds LVS anymore.

The log window has the following warning messages.

"
Running simulation in directory: "/home/aa/ugrad/billhung/ee141/LVS".

Begin netlist: Mar 29 17:36:20 2006
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "sram"
cell name = "predecoder_array_final"
view name = "extracted"
globals lib = "basic"
Running Artist Flat Netlisting ...
End netlist: Mar 29 17:36:20 2006

Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
146 nodes merged into 146 nodes

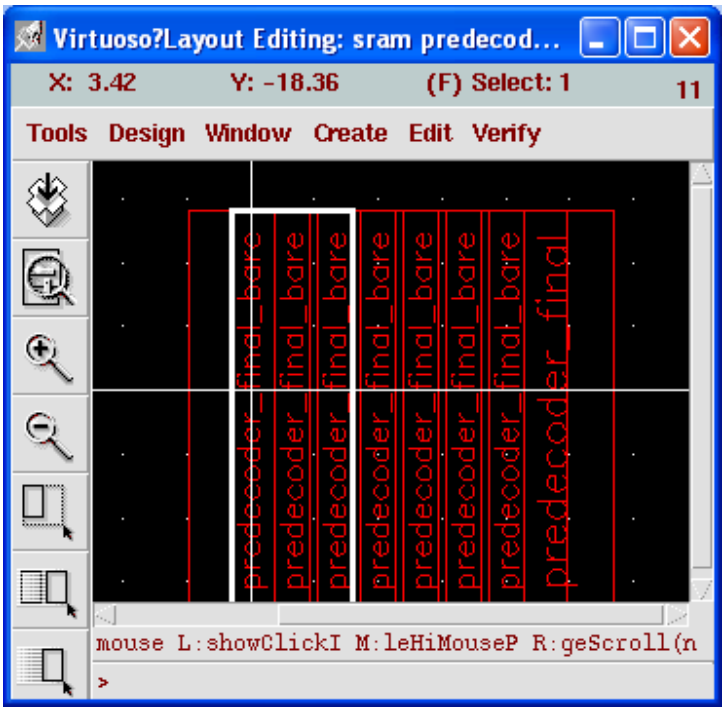
Begin netlist: Mar 29 17:36:20 2006
view name list = ("auLvs" "schematic")
stop name list = ("auLvs")
library name = "sram"
cell name = "predecoder_array_final"
view name = "schematic"
globals lib = "basic"
Running Artist Flat Netlisting ...
WARNING Couldn't get a write lock for
"/home/aa/ugrad/billhung/ee141/LVS/schematic/map/current"
Malformed Lock-Stake file.
WARNING XXopen: failed to lock file
/home/aa/ugrad/billhung/ee141/LVS/schematic/map/current in A_MODE mode - is
currently not locked.

global error:
Unable to create /home/aa/ugrad/billhung/ee141/LVS/schematic/map/current
file
si: Netlist did not complete successfully.
WARNING failed to open map file
"/home/aa/ugrad/billhung/ee141/LVS/schematic/map/current"
End netlist: Mar 29 17:36:20 2006

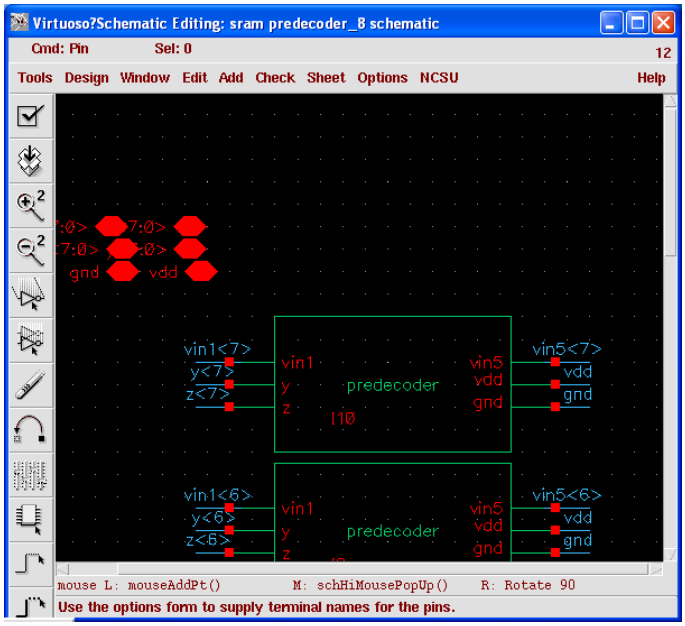
Comparison program did not complete.
"
What was the problem?

Just delete the whole LVS folder. Or find the file described in the warning, and delete the lock file., or files that has an old timestamp.

Predecoder (8 Instants)



Layout=sram/predecoder_8/layout



Schematic = sram/predecoder_8/schematic

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
74	nets
0	terminals
64	pmos
64	nmos

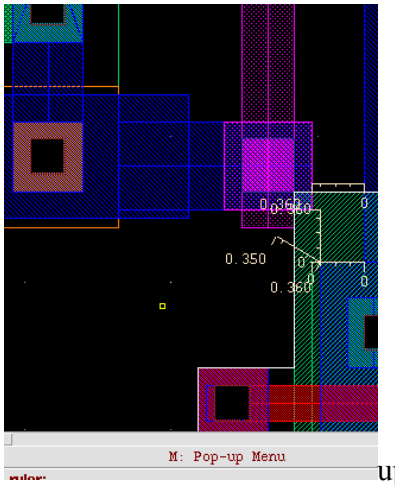
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
74	nets
34	terminals
48	pmos
48	nmos

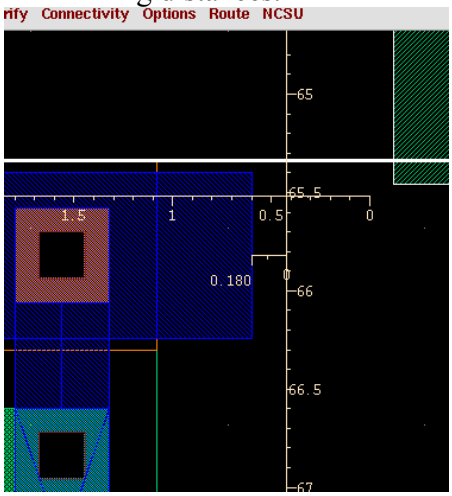
16 net-list ambiguities were resolved by random selection.

The net-lists match.

Minimizing Distance between Predecoder and Postdecoder



upper left=predecoder stage, lower right =postdecoderstage. Minimizing distances.



Matching Pitches with the 2 predecoder stages. Lower left predecoder, upper right postdecoder.

LVS Failed Error Again

Deleted all zero bytes files in
/home/aa/ugrad/billhung/ee141/sram/sram/decoder_final/schematic

WARNING Couldn't get a write lock for
"/home/aa/ugrad/billhung/ee141/LVSnew/layout/map/current"
Malformed Lock-Stake file.
WARNING XXopen: failed to lock file
/home/aa/ugrad/billhung/ee141/LVSnew/layout/map/current in A_MODE mode - is currently not locked.

global error:
Unable to create /home/aa/ugrad/billhung/ee141/LVSnew/layout/map/current file
si: Netlist did not complete successfully.

WARNING failed to open map file
"/home/aa/ugrad/billhung/ee141/LVSnew/layout/map/current"
End netlist: Mar 31 00:59:43 2006

Comparison program did not complete.

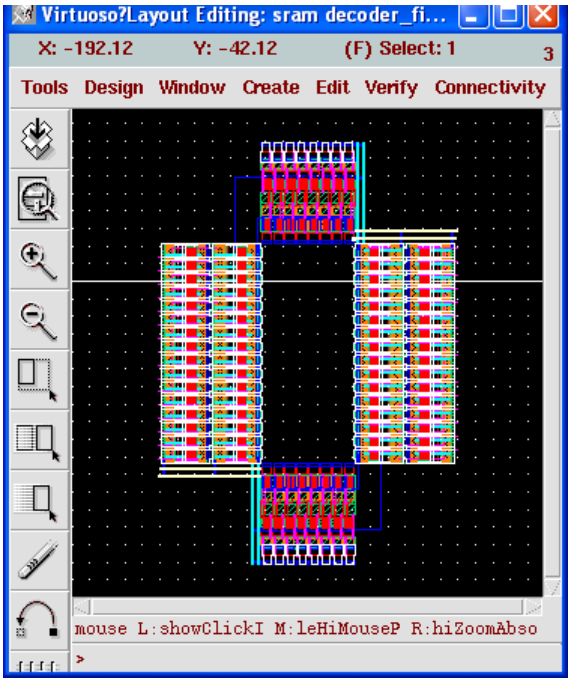
Deleted all zero bytes files in
/home/aa/ugrad/billhung/ee141/LVSnew/layout/map/current

Cellview (decoder_final layout) from lib (sram) is saved in the panic file
(/home/aa/ugrad/billhung/ee141/sram/sram/decoder_final/layout/layout.cd-)
To recover do:
dbOpenPanicCellView("sram" "decoder_final" "layout")
All the saved panic files were logged in panic.log in your home directory

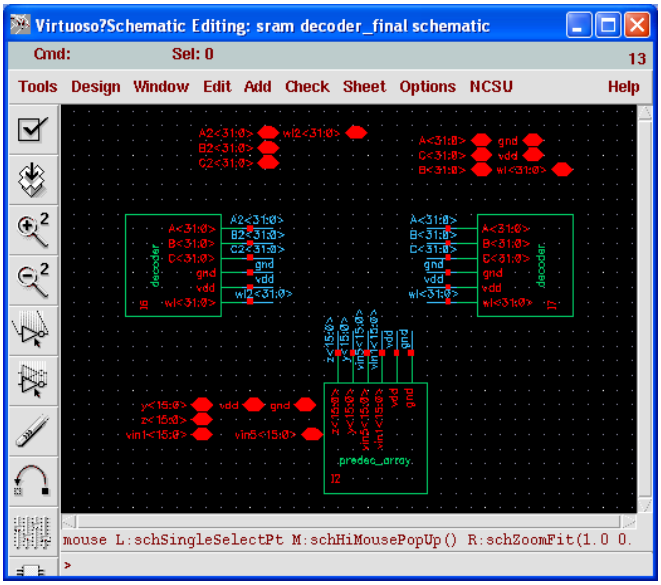
[1] Segmentation fault icfb

Solved the problem by not using the 32x32 SRAM array.

16-Postdecoder + 64-Predecoder



Layout=sram/decoder_final/layout



Schematic=sram/decoder_final/schematic

LVS Results

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist

count	
594	nets
0	terminals
512	pmos
512	nmos

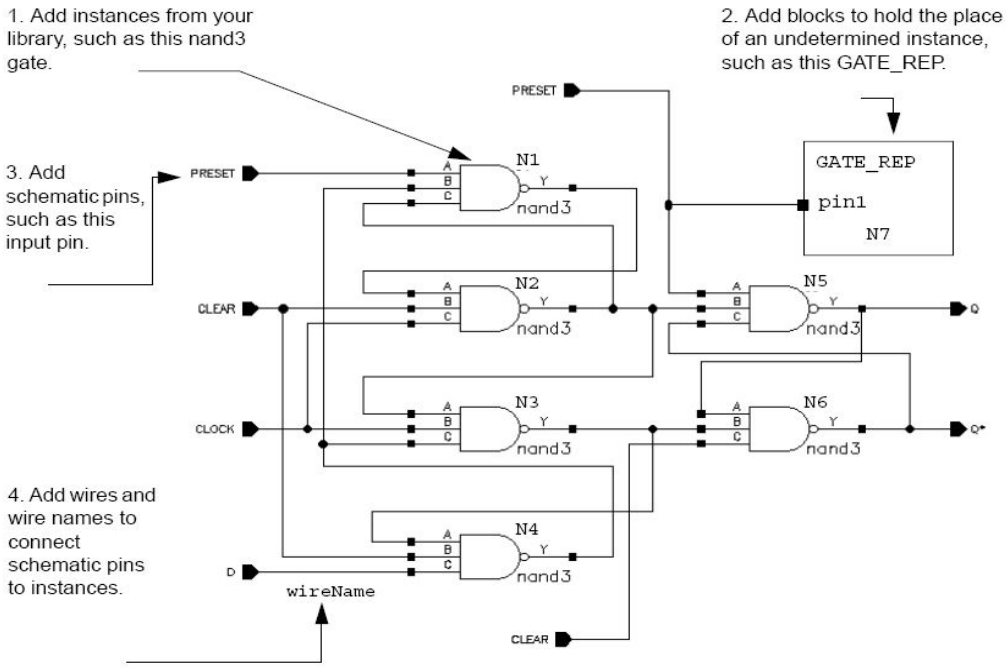
Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist

count	
594	nets
322	terminals
352	pmos
352	nmos

224 net-list ambiguities were resolved by random selection.

The net-lists match.

Wire Branching Examples



Use the suffix repeat operator `<*n>` to repeat each bit in a group of bit names before
expanding the vector term. For example, the following three names all describe the same
six-bit wire:

```
A<0:2*2>
A<0*2,1*2,2*2>
A<0,0,1,1,2,2
```