Dynamic Logic
Table of contents

Finding Sizing for 5-stage Dynamic Logic

Dynamic Logic chain with 3fF-not-nand-not-nand-not-cload. Try to find the sizing for HSPICE simulation.

Matlab Code

```
% Dynamic Logic
% 3fF-NOT-NAND-NOT-NAND-NOT-Cload
%Parameters
g1=1; g2=5/3; g3=1; g4=5/3; g5=1;
b1=1; b2=4; b3=1; b4=8; b5=1;
nstage=5;
%find cload
cw=5.5; %from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32
%Find h
G=g1*g2*g3*g4*g5; B=b1*b2*b3*b4*b5; F=(cload)/(3*cg);
H=G*B*F
h=H^(1/nstage)
%Find f
f(1)=h/(b1*g1);
f(2)=h/(b2*g2);
f(3)=h/(b3*g3);
f(4)=h/(b4*g4);
f(5)=h/(b5*g5);
s(5)=(cload)/f(5);  s(4)=s(5)/f(4);
s(3)=s(4)/f(3);  s(2)=s(3)/f(2);
s(1)=s(2)/f(1)


% add cw1
g1=1; g2=1; g3=5/3; g4=1;
b1=1; b2=4; b3=1; b4=1;
nstage2=4;
cw1=1.8641; %from HSPICE
cload = s(5)*8+cw1;
F2 = (cload)/(3*cg);
   %cw1 is M4 of the predecoder = 1.8641
B2= b1*b2*b3*b4;
G2 = g1*g2*g3*g4;
H2 = F2* G2* B2
h2 = H2^(1/nstage2)
f1(1)=h2/(b1*g1);
f1(2)=h2/(b2*g2);
f1(3)=h2/(b3*g3);
f1(4)=h2/(b4*g4);
s1(4)=(cload)/f1(4);
s1(3)=s1(4)/f1(3);
s1(2)=s1(3)/f1(2);
s1(1)=s1(2)/f1(1);
%get w
```



```
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
inv_min = 3*cg;
nand3_min = 5*cg;
w(5)=s(5)/nand3_min;
w(4)=s1(4)/inv_min;
w(3)=s1(3)/nand3_min;
w(2)=s1(2)/inv_min;
w(1)=s1(1)/inv_min
```

Matlab Result

```
cload =   52.9624
H =  2.1160e+003
h =    4.6249
s =  Columns 1 through 2
    2.2248   10.2895
  Columns 3 through 4
    7.1383   33.0139
  Column 5
   11.4515
H2 =  280.1037
h2 =
    4.0910
w =
  Columns 1 through 2
    1.0000    4.0910
  Columns 3 through 4
    2.5104   10.2702
  Column 5
    3.0883
```

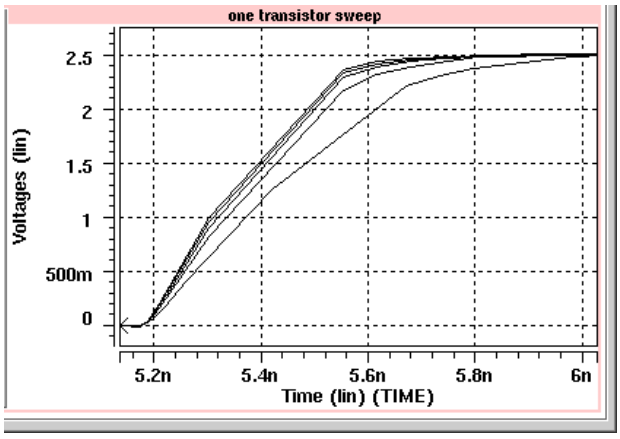
Sweeping Transistor – NAND Gate Test

Trying to sweep logic gate sizes in HSPICE.

HSPICE Code

```
one transistor sweep
.lib '/home/ff/ee141/MODELS/g25.mod' TT
****************************************
* Parameter
****************************************
.param vddp = 2.5
.param wnmin='0.36u'
.param wpmin='2*wnmin'
.param multiplier = 2.0449
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************
.subckt NAND3 Vdd Gnd VinA VinB VinC Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w='wpmin'
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w='wpmin'
Mp3 Vout VinC Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vmid1 VinA Gnd Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid2 VinB Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vout VinC Vmid2 Gnd nmos l=0.24u w='wnmin*3'
.ends

xnand vdd 0 vin1 vdd vdd vout  NAND3 M=multiplier
cout vout 0 13f
****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op
.tran 0.05ns 10ns sweep multiplier 1 5 1
.end
```

Awave Result



Sweeping Transistor – NAND Gate with subcircuit

Sweep one NAND gate with subcircuit in another file.

Sweep_transistor.sp

```
one transistor sweep

.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc 'gate.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param wnmin='0.36u'
.param wpmin='2*wnmin'
.param multiplier = 2.0449
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************

xnand vdd 0 vin1 vdd vdd vout  NAND3 M='multiplier'
cout vout 0 13f

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op


.tran 0.05ns 10ns sweep multiplier 1 5 1
.end
```

Sweep_transistor.sp

```
one transistor sweep

.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc 'gate.sp'
```

```
****************************************
* Parameter
****************************************
.param vddp = 2.5
.param wnmin='0.36u'
.param wpmin='2*wnmin'
.param multiplier = 2.0449
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************

xnand vdd 0 vin1 vdd vdd vout  NAND3 M='multiplier'
cout vout 0 13f

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op


.tran 0.05ns 10ns sweep multiplier 1 5 1
.end
```

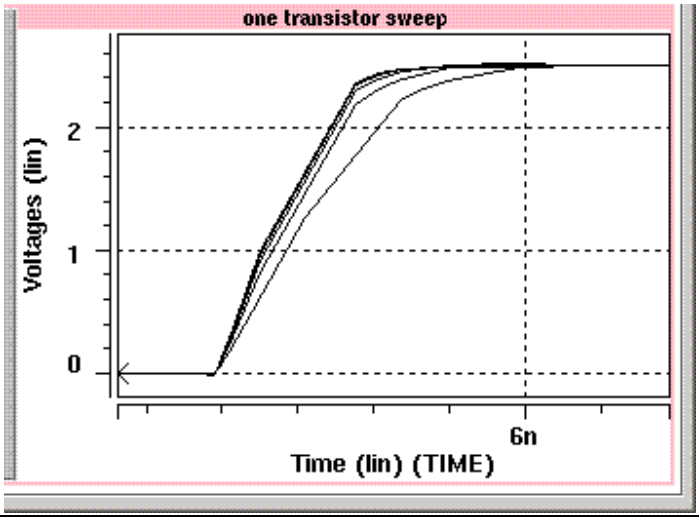
Gate.sp

```
.param wnmin='0.36u'
.param wpmin='2*wnmin'

.subckt INV vin vout vdd vss
M1 vout vin vss vss  nmos l=0.24u w='wnmin'
M2 vout vin vdd vdd  pmos l=0.24u w='wpmin'
.ends

.subckt NAND3 Vdd Gnd VinA VinB VinC Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w='wpmin'
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w='wpmin'
```



```
Mp3 Vout VinC Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vmid1 VinA Gnd Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid2 VinB Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vout VinC Vmid2 Gnd nmos l=0.24u w='wnmin*3'
.ends

.subckt Sram Vdd Gnd vword vbit vbitbar
   *M<name> <drain> <gate> <source> <bulk> <model> <geometry>
M0 2 5 Vdd Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M1 Vdd 2 5 Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M2 2 5 0 0 nmos L=240E-9 W=480E-9 AD=165.599996280845E-15
+AS=288.000011209114E-15 PD=779.999993483216E-9 PS=1.67999996847357E-6
M=1
M3 0 2 5 0 nmos L=240E-9 W=480E-9 AD=288.000011209114E-15
+AS=165.599996280845E-15 PD=1.67999996847357E-6 PS=779.999993483216E-9
M=1
M4 vbit vword 2 0 nmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9
M=1
M5 5 vword vbitbar 0 nmos L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6
M=1
.ends


.subckt NOR Vdd Gnd VinA VinB Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w=0.6u
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w=0.6u
Mn1 Vout VinA vmid Gnd nmos l=0.24u w=0.72u
Mn2 vmid VinB Gnd Gnd nmos l=0.24u w=0.72u
.ends
```

Awave Result



Paramters

Cw = 12.60438 fF
Cw1 = 1.8641f
SRAM pitch = 1.92um
PMOS-NMOS ratio: 1.6 (Rabaey, 209)

Sweeping Static Logic Transistors

The goal is the find the optimal delay by sweeping the width of transistors used in the decoder circuit.

Sweep Static Logic HSPICE

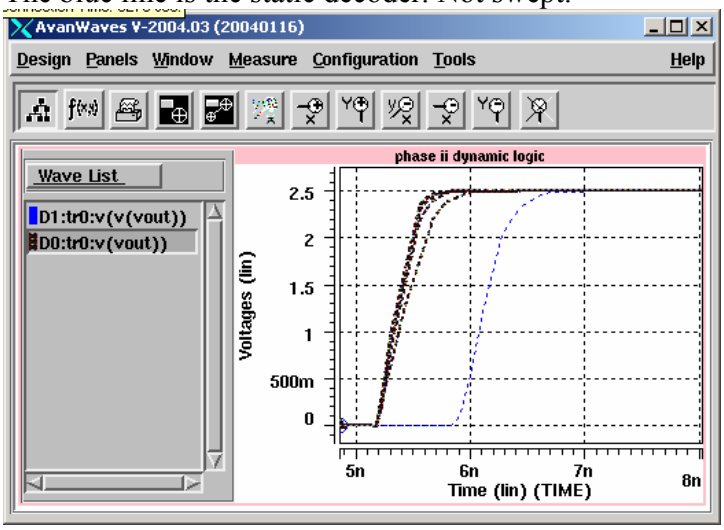
```
PHASE II DYNAMIC LOGIC
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'logic.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_nand1 = 4.09
.param multi_inv2 = 2.51
.param multi_nand3 = 10.27
.param multi_inv3 = 3.0
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************
xinv1 vin1 vin2 vdd 0 INV
xnand1_b1 vdd 0 vdd vdd vin2 vin3 NAND3 M='multi_nand1'
xnand1_b2 vdd 0 0 0 vin2 x NAND3 M='multi_nand1'
xnand1_b3 vdd 0 0 0 vin2 y NAND3 M='multi_nand1'
xnand1_b4 vdd 0 0 0 vin2 z NAND3 M='multi_nand1'
xinv2 vin3 vin4 vdd 0 INV M='multi_inv2'
cw1 vin5 0 1.8641f
xnand2_b1 vdd 0 vdd vdd vin4 vin5 NAND3 M='multi_nand3'
xnand2_b2 vdd 0 0 0 vin5 a NAND3 M='multi_nand3'
xnand2_b3 vdd 0 0 0 vin5 b NAND3 M='multi_nand3'
```

```
xnand2_b4 vdd 0 0 0 vin5 c NAND3 M='multi_nand3'
xnand2_b5 vdd 0 0 0 vin5 d NAND3 M='multi_nand3'
xnand2_b6 vdd 0 0 0 vin5 e NAND3 M='multi_nand3'
xnand2_b7 vdd 0 0 0 vin5 f NAND3 M='multi_nand3'
xnand2_b8 vdd 0 0 0 vin5 g NAND3 M='multi_nand3'
xinv3 vin5 vout vdd 0 INV M='multi_inv3'
cload vout 0 12.60438fF

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
cout vout 0 13f

**************************************
* Analysis
```

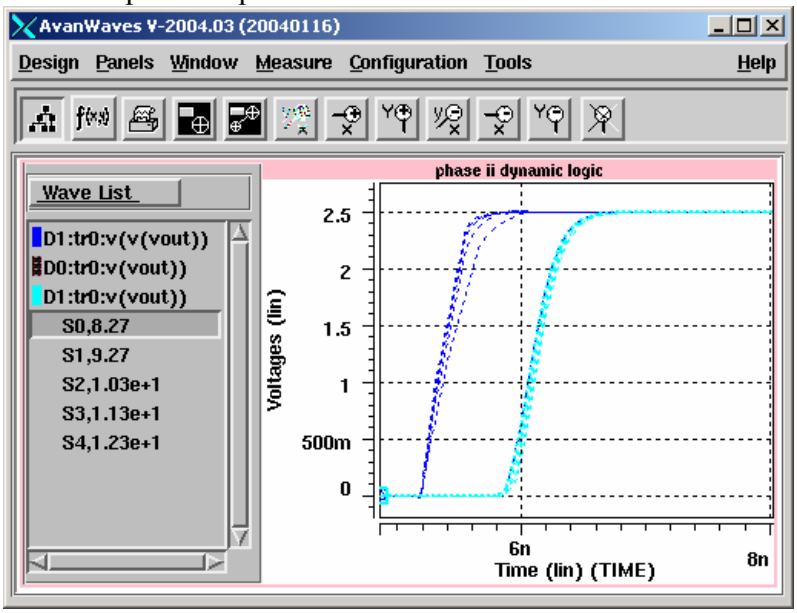
```
**************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op

.tran 0.01ns 11ns sweep multi_nand3 9.27 11.27 1 sweep multi_nand1 3.09 5.09 1 sweep
multi_inv3 3.09 5.09 1
.meas tran tplh trig V(vin1) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1
.end
```

Awave Code

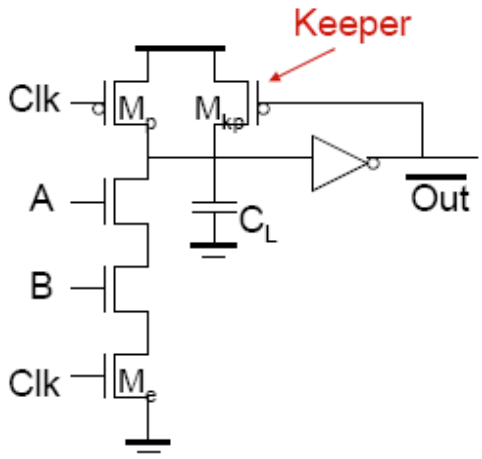
The blue line is the static decoder. Not swept.



The multiplier swept.

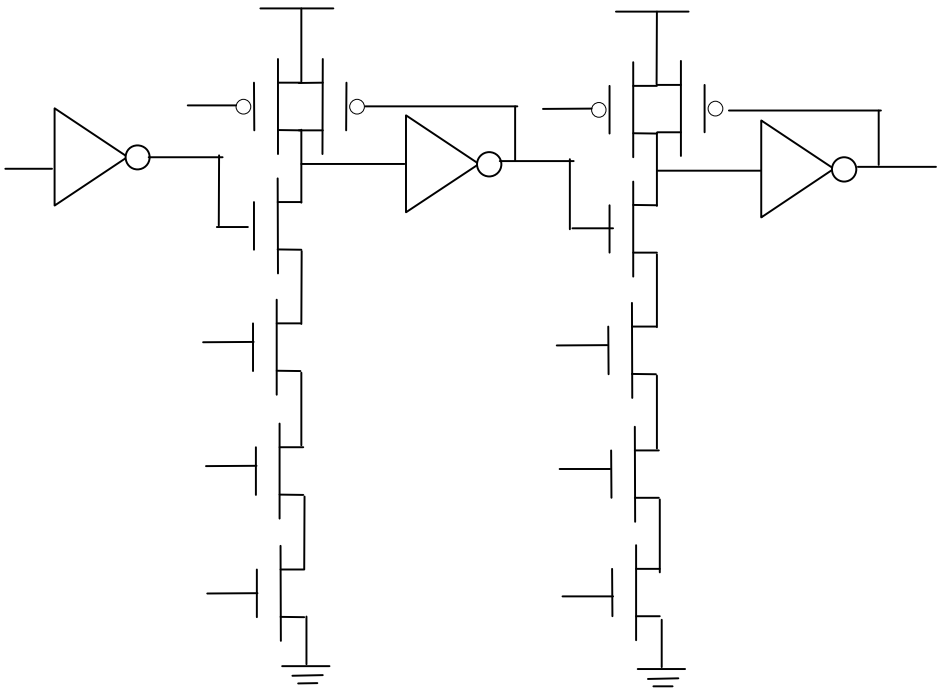


Dynamic Logic Gates



2-input-NAND with inverter [Nikolic, Lecture 19, page 12]

3fF-NOT-NAND-NOT-NAND-NOT-Cload dynamic circuit



5-Stage Dynamic Logic that Does Not Work

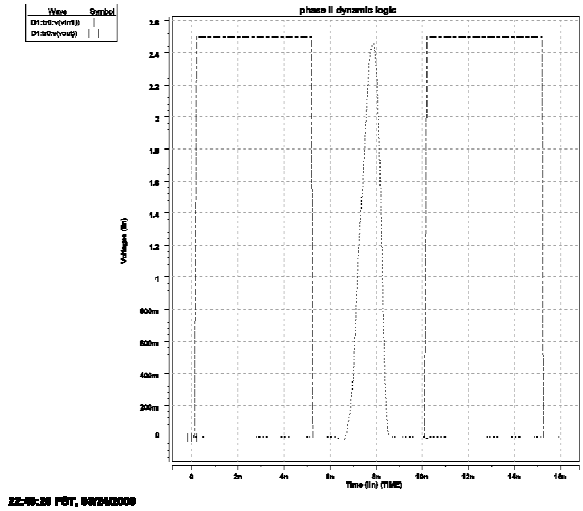
The problem with 5-stages is when all inputs are on, the output oscillate between vdd and zero. This is not suitable for a decoder.

HSPICE

```
PHASE II DYNAMIC LOGIC
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'gate.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_nand1 = 4.09
.param multi_inv2 = 2.51
.param multi_nand3 = 10.27
.param multi_inv3 = 3.0
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin1 0 pulse(0v 2.5v 0.1n 0.1n 50ps 5ns 10ns)
Vclk clk 0 pulse(0v 2.5v 0.1n 0.1n 50ps 2.5ns 5ns)
****************************************
* Netlist
****************************************
xinv1 vin1 vin2 vdd 0 INV
xnand1_b1 vdd 0 vin2 vin2 vin2 vin3 clk vin4 DNAND3 M='multi_nand1'
xnand1_b2 vdd 0 0 0 vin2 x clk xx  DNAND3 M='multi_nand1'
xnand1_b3 vdd 0 0 0 vin2 y clk yy DNAND3 M='multi_nand1'
xnand1_b4 vdd 0 0 0 vin2 z clk zz  DNAND3 M='multi_nand1'
xinv2 vin3 vin4 vdd 0 INV M='multi_inv2'
cw1 vin5 0 1.8641f
xnand2_b1 vdd 0 vin4 vin4 vin4 vin5 clk vout DNAND3 M='multi_nand3'
xnand2_b2 vdd 0 0 0 vin5 a clk aa DNAND3 M='multi_nand3'
xnand2_b3 vdd 0 0 0 vin5 b clk bb DNAND3 M='multi_nand3'
xnand2_b4 vdd 0 0 0 vin5 c clk cc DNAND3 M='multi_nand3'
xnand2_b5 vdd 0 0 0 vin5 d clk dd DNAND3 M='multi_nand3'
xnand2_b6 vdd 0 0 0 vin5 e clk ee DNAND3 M='multi_nand3'
xnand2_b7 vdd 0 0 0 vin5 f clk ff DNAND3 M='multi_nand3'
xnand2_b8 vdd 0 0 0 vin5 g clk gg DNAND3 M='multi_nand3'
xinv3 vin5 vout vdd 0 INV M='multi_inv3'
cload vout 0 12.60438fF

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
```

```
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
cout vout 0 13f

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op

.tran 0.1ns 16ns *sweep multi_nand3
.meas tran tplh trig V(vin1) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1
.end
```

Awaves



6-Stage Dynamic Logic

6 Stage Dynamic Logic will have the output oscillating during a read. However, for a decoder design, we need to have the output stay high for multiple cycles.

HSPICE

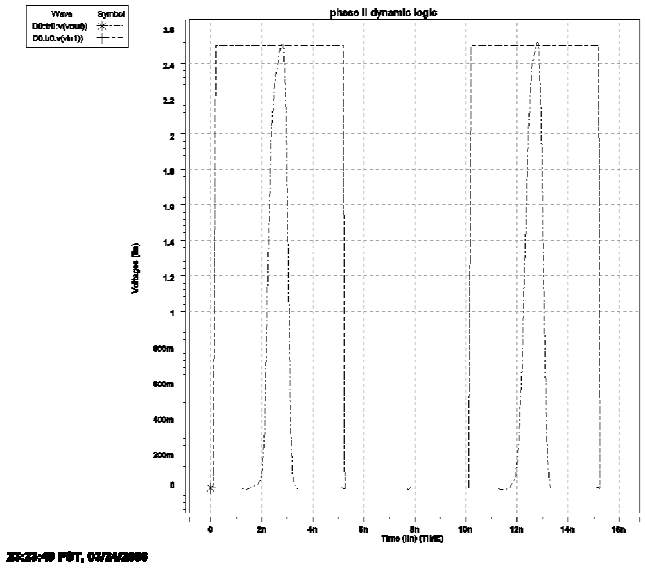
```
PHASE II DYNAMIC LOGIC
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'gate.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_nand1 = 4.09
.param multi_inv2 = 2.51
.param multi_nand3 = 10.27
.param multi_inv3 = 3.0
.param multi_inv4 = 4.6
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin1 0 pulse(0v 2.5v 0.1n 0.1n 50ps 5ns 10ns)
Vclk clk 0 pulse(0v 2.5v 0.1n 0.1n 50ps 2.5ns 5ns)
****************************************
* Netlist
****************************************
xinv1 vin1 vin2 vdd 0 INV
xinv2 vin2 vin3 vdd 0 INV M='multi_inv2'
xnand1_b1 vdd 0 vin3 vin3 vin3 vin4 clk vin5 DNAND3 M='multi_nand1'
xnand1_b2 vdd 0 0 0 vin3 x clk xx  DNAND3 M='multi_nand1'
xnand1_b3 vdd 0 0 0 vin3 y clk yy DNAND3 M='multi_nand1'
xnand1_b4 vdd 0 0 0 vin3 z clk zz  DNAND3 M='multi_nand1'
```

```
xinv3 vin4 vin5 vdd 0 INV M='multi_inv3'
cw1 vin5 0 1.8641f
xnand2_b1 vdd 0 vin5 vin5 vin5 vin6 clk vout DNAND3 M='multi_nand3'
xnand2_b2 vdd 0 0 0 vin5 a clk aa DNAND3 M='multi_nand3'
xnand2_b3 vdd 0 0 0 vin5 b clk bb DNAND3 M='multi_nand3'
xnand2_b4 vdd 0 0 0 vin5 c clk cc DNAND3 M='multi_nand3'
xnand2_b5 vdd 0 0 0 vin5 d clk dd DNAND3 M='multi_nand3'
xnand2_b6 vdd 0 0 0 vin5 e clk ee DNAND3 M='multi_nand3'
xnand2_b7 vdd 0 0 0 vin5 f clk ff DNAND3 M='multi_nand3'
xnand2_b8 vdd 0 0 0 vin5 g clk gg DNAND3 M='multi_nand3'
xinv4 vin6 vout vdd 0 INV M='multi_inv4'
cload vout 0 12.60438fF

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
cout vout 0 13f

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op
```

```
.tran 0.1ns 16ns *sweep multi_nand3
.meas tran tplh trig V(vin1) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1
.end
```

Awaves

6-Stage not-not-nand-not-nand-not circuit Transcient Plot



Conclusion. Dynamic is not suitable for the decoder we need.