UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EECS 141: Digital Integrated Circuits - Spring 2006

Report Cover Sheet

TERM PROJECT: SRAM Design Cover Sheet

Report 3 – SRAM bitline design

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	GRADE
Approach, result and correctness (70%)	
Report (30%)	
TOTAL	

Schematic and Layout of the Bitline

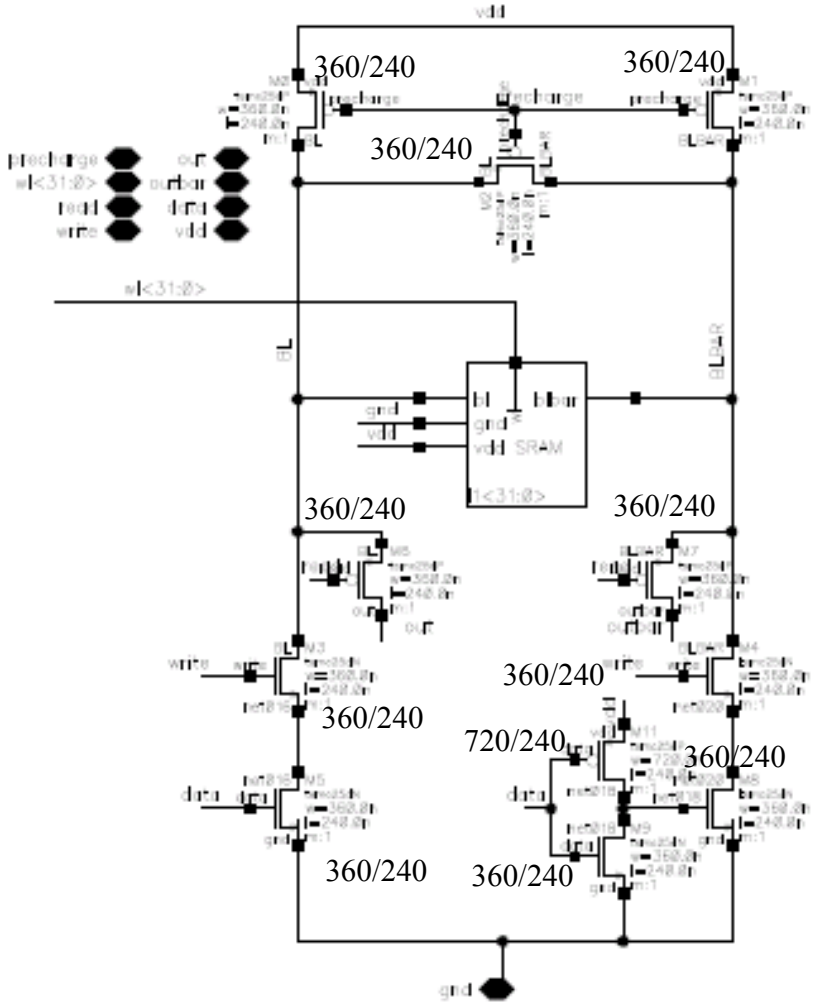

Figure 1: Bitline Schematic

Figure 2: Cadence Bitline Layout

(right) This is the bitline schematic, the sense amp is connected to the out and !out of the bitline schematic. All the transistors, except the pmos of the data line inverter, are minimum sized. (left) The layout of one bitline column with peripheral circuitry. Since we use metal 3 for bitline and !bitline, the wire capacitance is neligible (<2fF). The wire capacitance was ignored by Cadence Layout Tool.

HSPICE Simulation Waveforms

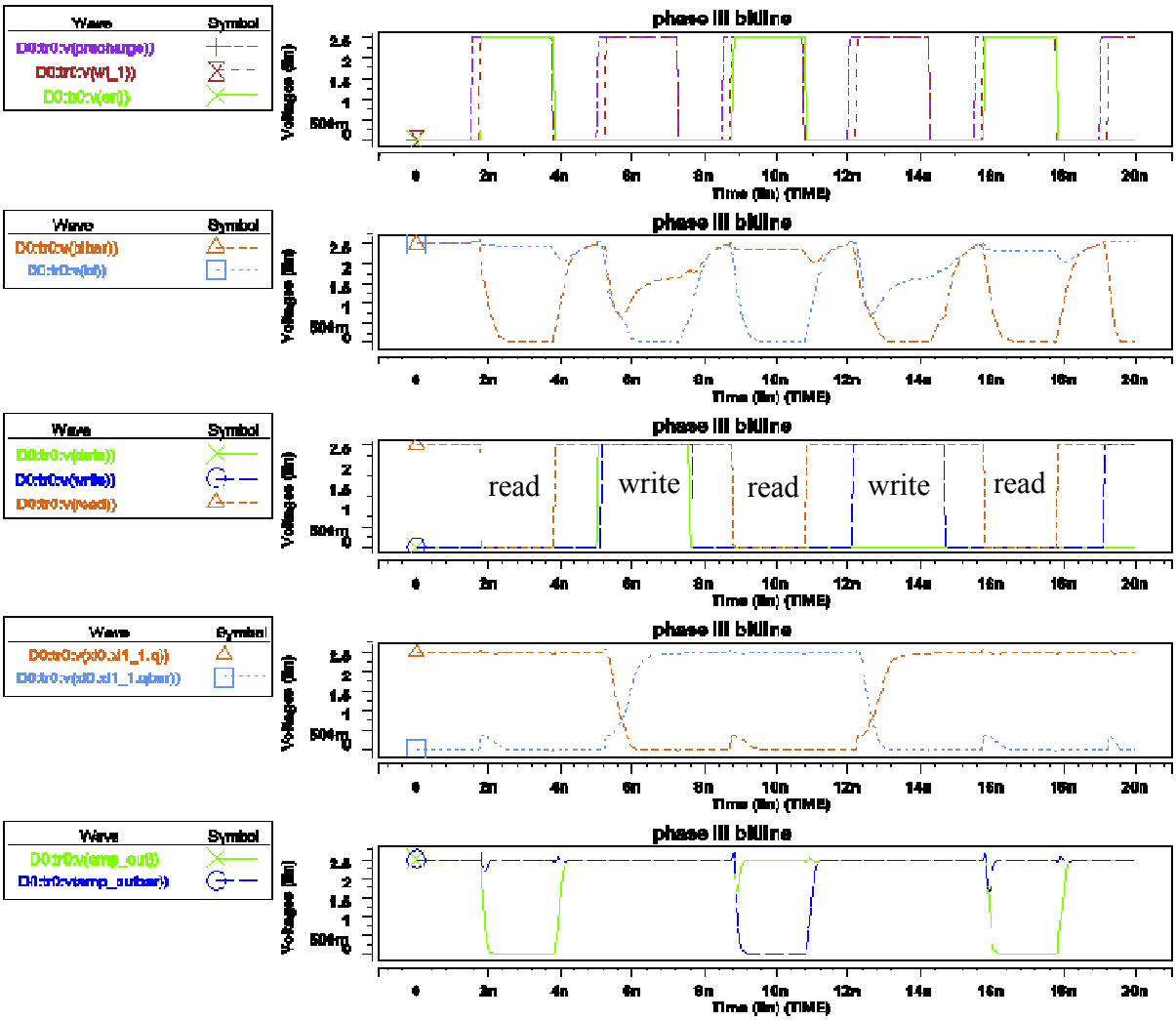

Figure 3: HSPICE Bitline and Sense Amp Simulation

1. The simulation starts with a read operation. The signals – precharge (active low), wl_1, and en (!read) –are asserted sequentially. The bit in the sram cell "q" is high, so the output of the sense amp "out" is low during the first read operation. Notice that the read signal is asserted when the voltage difference between the bitline signals, "bl" and "blbar", is slightly larger than 100mV.
2. Then a write operation writes a zero in "q ". The signals – precharge (not required in a write operation), data, write, and wl_1 –are asserted sequentially. Notice that right after precharge, "bl" is going to zero, and "blbar" is lowered to about one third of V_{dd} because of charge sharing. Writing a zero into "q" will pull "bl" to ground and pull "blbar" up to $V_{dd} - V_T$.
3. The second read operation sucessfully read the zero from "q", and the output of the sense amp "outbar" is brought down to zero.
4. The second write operation writes a zero into "qbar".
5. Final read operation sucessfully read the one from "q", and "out" is brought down to zero.

Sense Amp Schematic

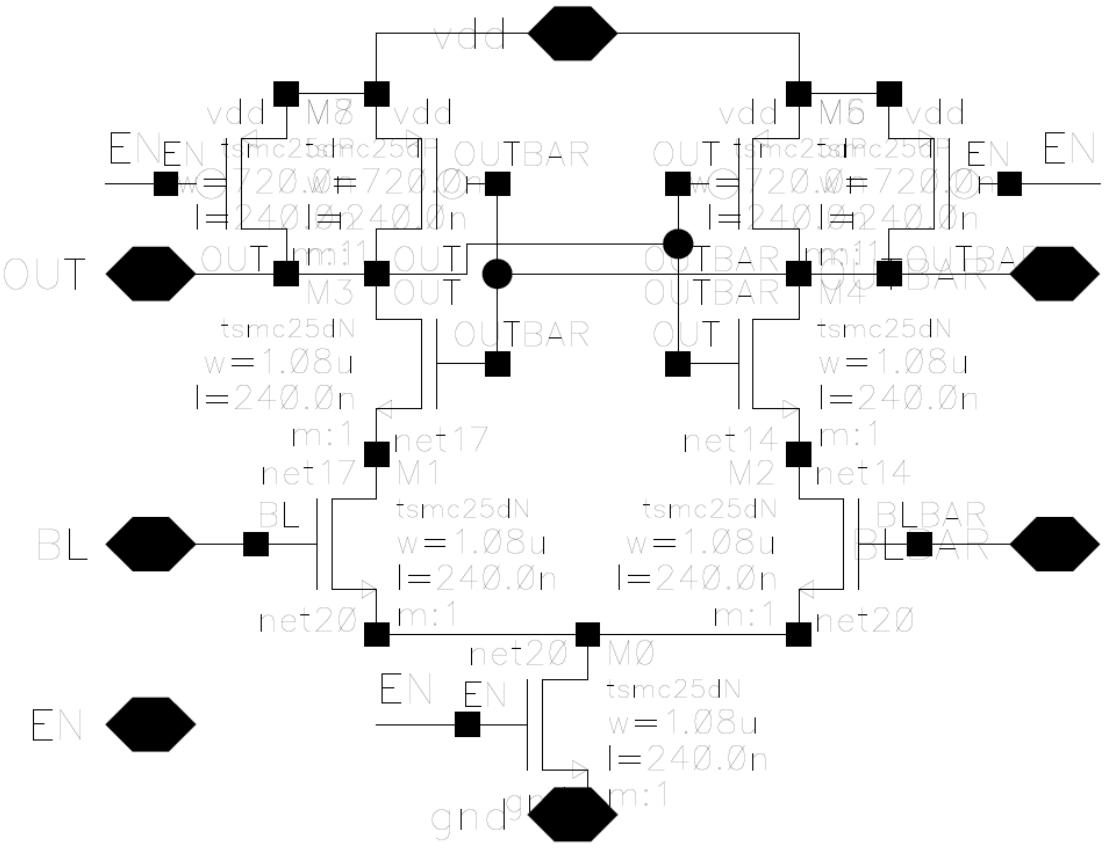

Figure 4: The Cadence schematic of one sense amp

The read operation simulation is shown in page 2. The enable signal "EN" is the negation of the "read" signal in the bitline circuit. The "BL" and "BLBAR" signals are connected to "out" and "outbar" signals in the bitline circuit. When the 100mV difference between the inputs of sense amp has been developed, the side with higher input voltage will be pulled down harder. The cross-coupled inverters provide the positive feedback to amplify the difference; the side with high input voltage will be pulled down to ground whereas the other side will be pulled up to V_{dd}.

Since the SRAM cells are small, they have a weaker pull-up strength, so we need to use a sense amp to improve it. The sizing of the Sense Amp is done with reference to a 2:1 Inverter so that both the pull-up and pull-down strength will be the same. In an actual design, the sense amp should be large to minimize the pull-up time. The maximum limit on the sense amp transistor sizes should be determined by doing the layout. That is to say the sense amp should be as large as the room available for the sense amp. However, since the layout of the sense amp was not required, the maximum size of the sense amp transistors cannot be determined. Therefore, the sense amp was only sized to 2 times the minimum size for the pmos and 3 times the minimum size for the nmos to meet the 2:1 ratio.