

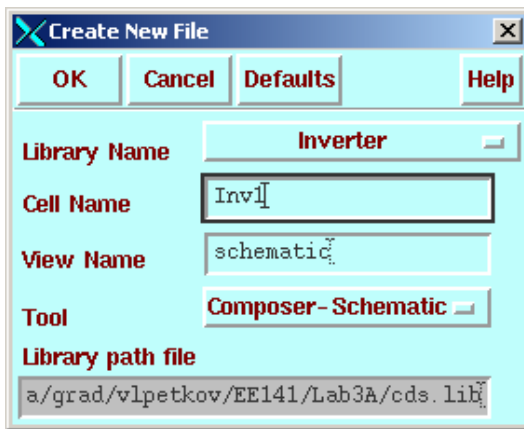
Schematics tutorial

Last Modified: February 14, 2006

Creating Schematic

(1) By this point you are in Cadence and have created a library Inverter and a layout cellview Inv1.

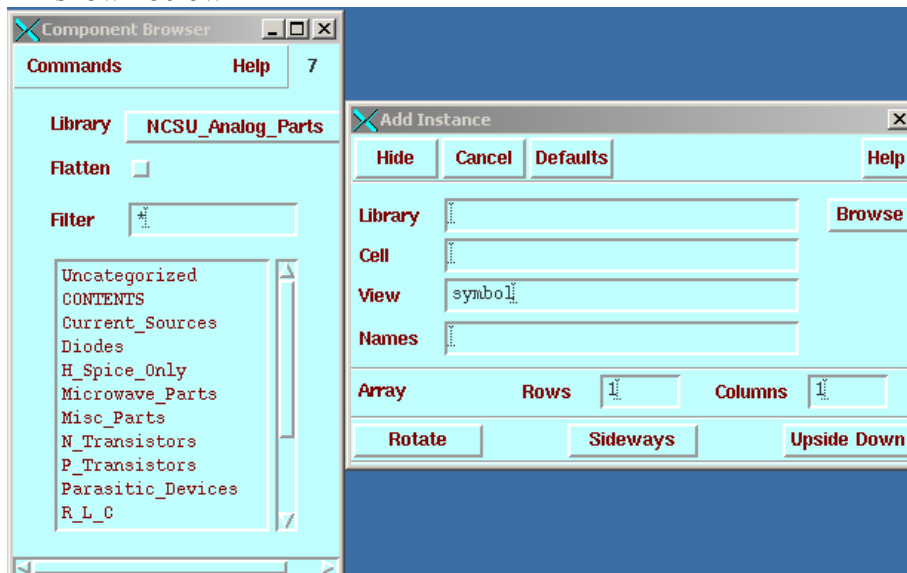
(2) Now create a schematic cell view using: File>New>Cell View. This will open up a new window. Choose the Inverter library and fill in the cell name with Inv1:



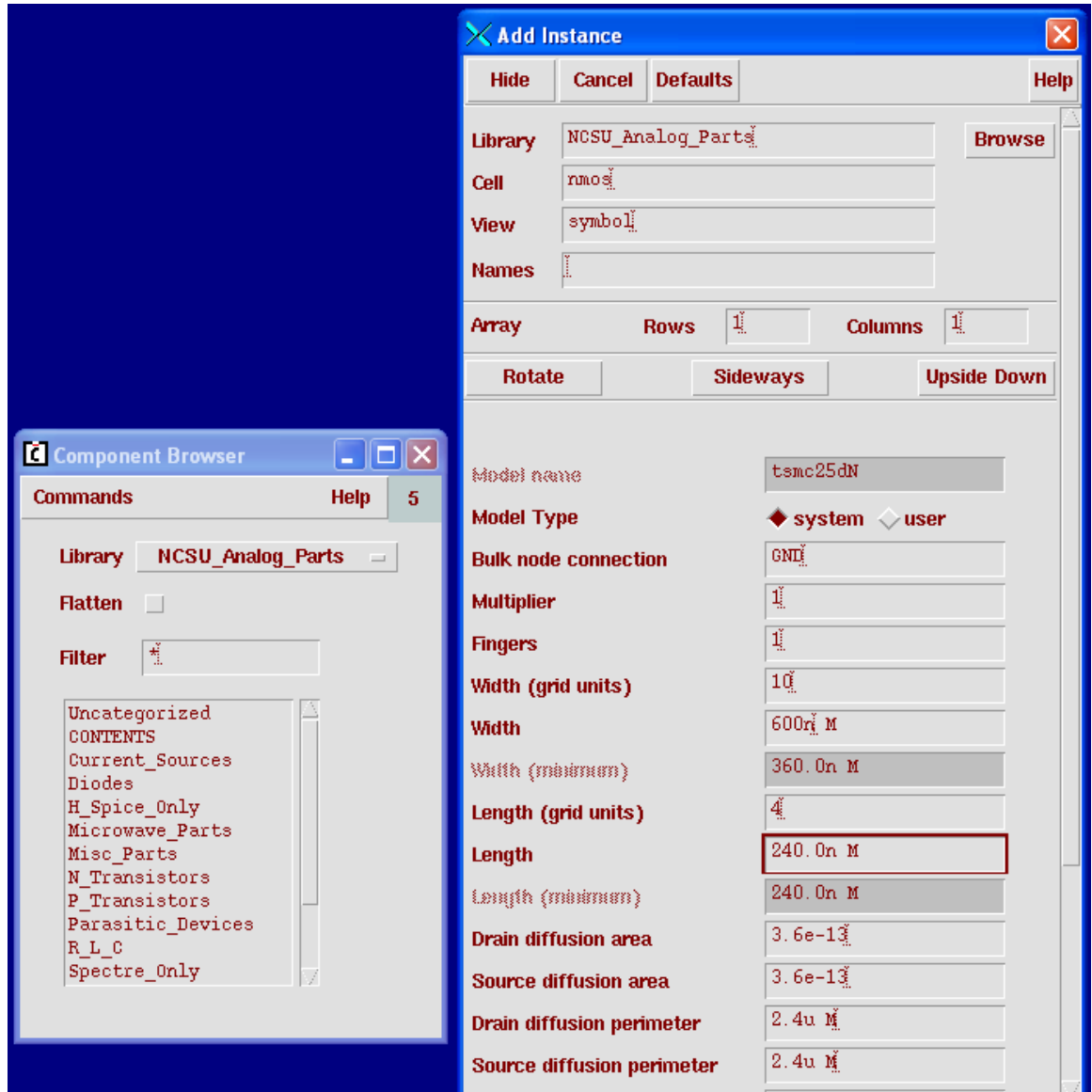
Then, click ok. This will open up a blank schematic window.

(3) Instantiate the transistor models from the library

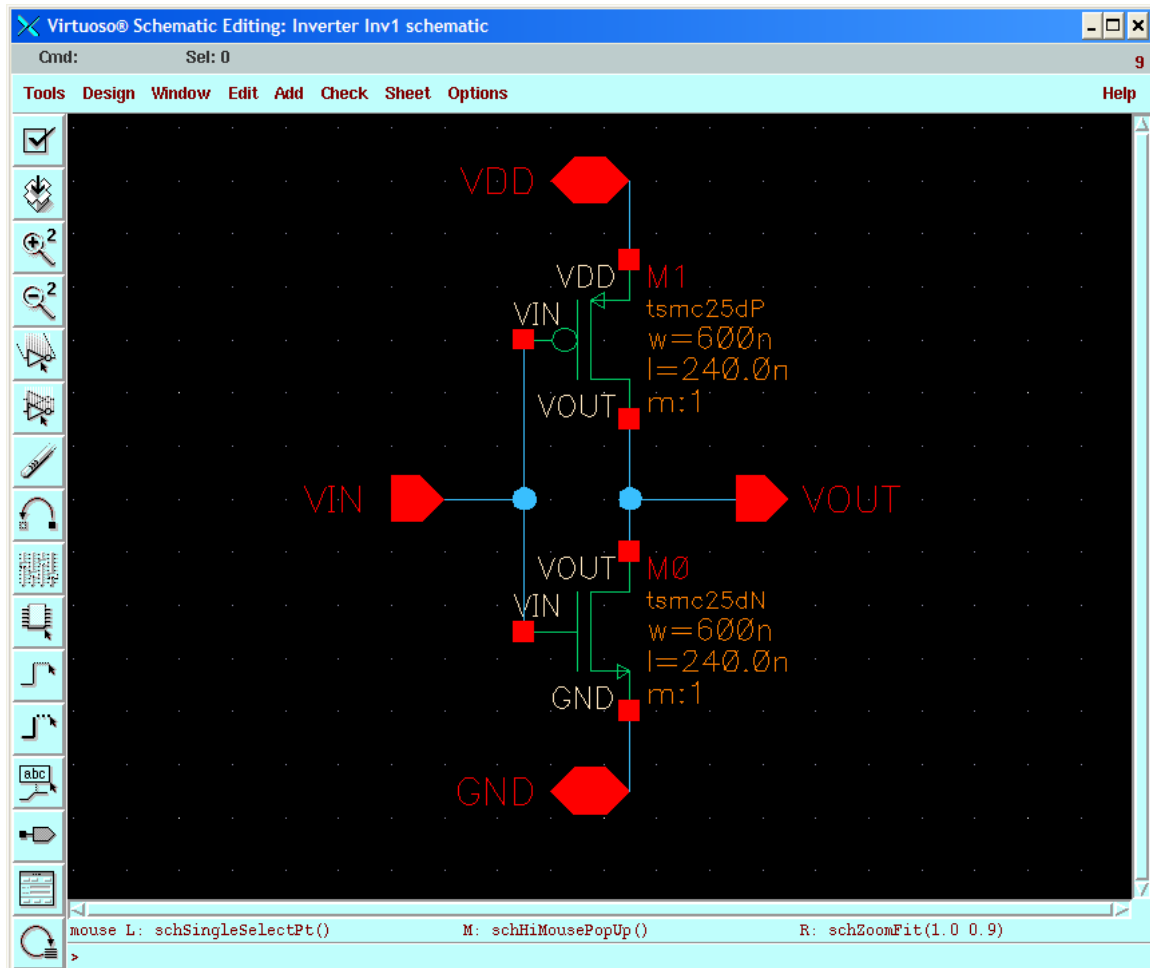
(a) Press “i” while the schematic window is active. (You can also use the pull down menu from the schematic window). This will bring up 2 windows as shown below



- (b) Choose the correct transistor model and fill the desired size. You can use either nmos or nmos4, the latter has an explicit Bulk node on the symbol. If you used nmos/pmos, make sure to change the “Bulk node connection” parameter to GND and VDD respectively, since we are labeling these nets with those names. Then click Hide and place the transistor in the schematic window.



- (c) After you have placed all device symbols down. You can use wires (hotkey **w**) to connect all the devices together to create an inverter as shown below. Use Add→Pin to put down input, output and supply pins that match the pins you created in the layout view.



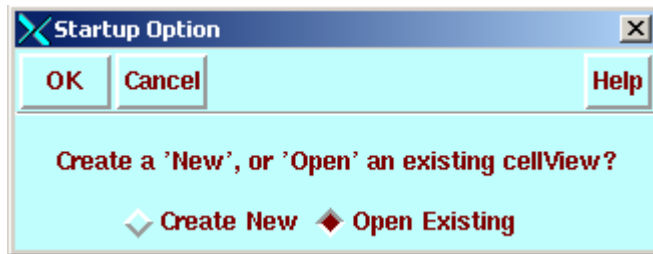
Cross Probing with Virtuoso Layout Editor and Schematic Composer

Once you have drawn both the layout and schematics, you can use the cross-probing function. This allows you to select a piece of layout and highlight the corresponding object in the schematic, or vice versa. You can initiate cross probing from either the Layout Editor or Schematic Composer.

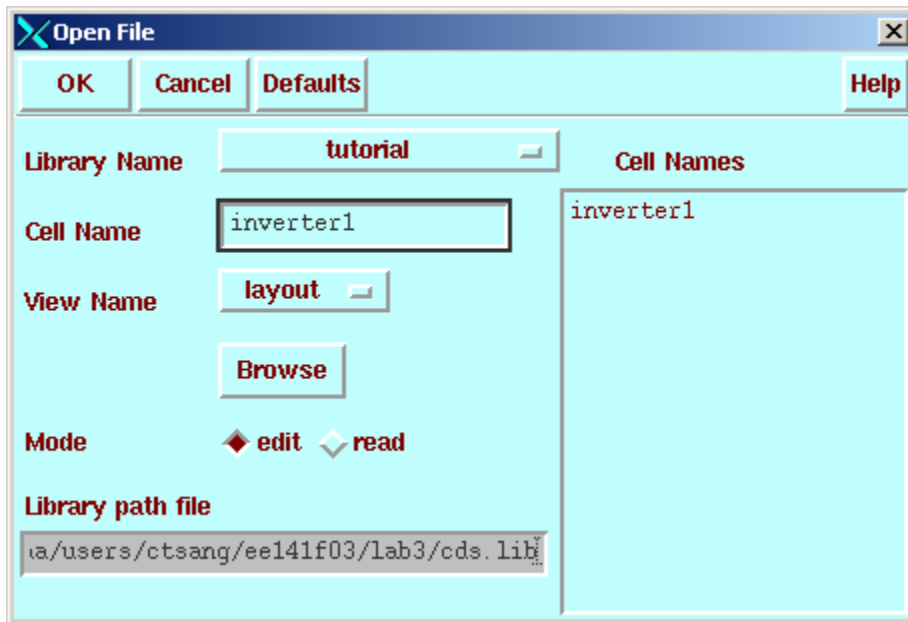
Tools Setup

(1) Setup Layout XL. This is a powerful tool that allows you to quickly check correspondence between schematic and layout views. In larger designs, Layout XL can be very useful in guiding you through layout based on an existing schematic.

→ Open the schematic in Composer and choose Tools → Design Synthesis → Layout XL from the menu.



→Click OK and the next window will ask you to choose the layout view



This will bring up side-by-side copies of your schematic and layout views. The layout window is sometimes called the “Layout XL” window, as this is where editing is most often done with this tool, but it is basically just the Virtuoso Layout Editor with some new options.

Cross-Probing

You can probe (highlight) objects while working in the schematic or layout editors. Note that probing an object removes the existing highlights. When you probe a pin or net in one view, it will be highlighted in the other view as well.

Cross-Probing from Virtuoso XL

With the Connectivity - Probe command, you can probe an object in the Virtuoso XL or Virtuoso schematic composer windows and highlight the object in the Virtuoso XL, Virtuoso schematic composer.

1. Choose Connectivity –XL Probe in the Virtuoso XL window.

Note: If you do not see this command in the menu, choose Tools - Virtuoso XL.

Optionally, press F3 to display the Virtuoso XL Probe Options form.

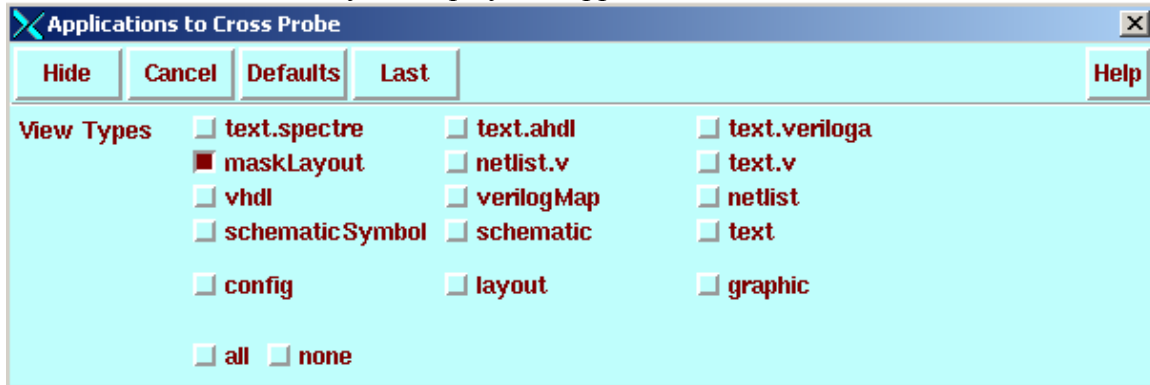
2. Click on a pin, net, or device in the Virtuoso XL or schematic composer window.

Cross-Probing from the Composer

You can use the composer Design - Probe - Add submenu commands to initiate cross-probing. Follow these steps:

1. In the Composer window, choose Add Net, Add Pin, or Add Instance from the Design - Probe menu.

2. Press F3, if necessary, to display the Applications to Cross Probe form.



3. Select the maskLayout view type.

4. Click in the schematic to place the probe. You will see both the schematic and corresponding layout highlighted.

Layout vs. Schematic (LVS) checking (Optional)

The DRC layout check that you are familiar with only checks to make sure that the shapes you drew are physically possible to manufacture. There is no guarantee that what you drew is actually the same circuit as what you have in your schematic. The LVS check is a tool that can analyze your layout and find all of the devices and connections between them, and then compare this to your schematic view. Even for small cells like an inverter it is necessary to run this check, because if there is a small error here it will turn into a lot of errors when you use the inverter cell in a larger design. This is one of the ways that hierarchical design can be used to help you by verifying your design in small, manageable sections. For larger cells, it is usually difficult to pass LVS the first time, which makes you realize how important a tool it is! Without LVS, you have almost no chance of ever getting a chip that works.

Running LVS

The LVS check is split into two parts (it seems silly, but there is a reason):

- 1) “Extracting” the layout. This is where the devices and connectivity are determined from your layout view.
- 2) “LVS” check, which actually compares the “extracted” view (not the layout view) against the schematic.

Extracting your layout

From the layout editor, choose Verify→Extract... and fill in the form as shown below.

The screenshot shows the 'Extractor' dialog box with the following settings:

- Extract Method:** flat (selected), macro cell, full hier, incremental hier
- Join Nets With Same Name:**
- Echo Commands:**
- Switch Names:** [Empty text box] **Set Switches** button
- Run-Specific Command File:**
- Inclusion Limit:** 1000
- View Names:** Extracted: extracted, Excell: excell
- Rules File:** divaEXT.rul
- Rules Library:** TechLib_tsmc03d
- Machine:** local (selected), remote, Machine: [Empty text box]

When extraction is complete it will print a message in the icfb window telling you how many devices it found (often a useful first check) and if there were any errors during the extraction process itself.

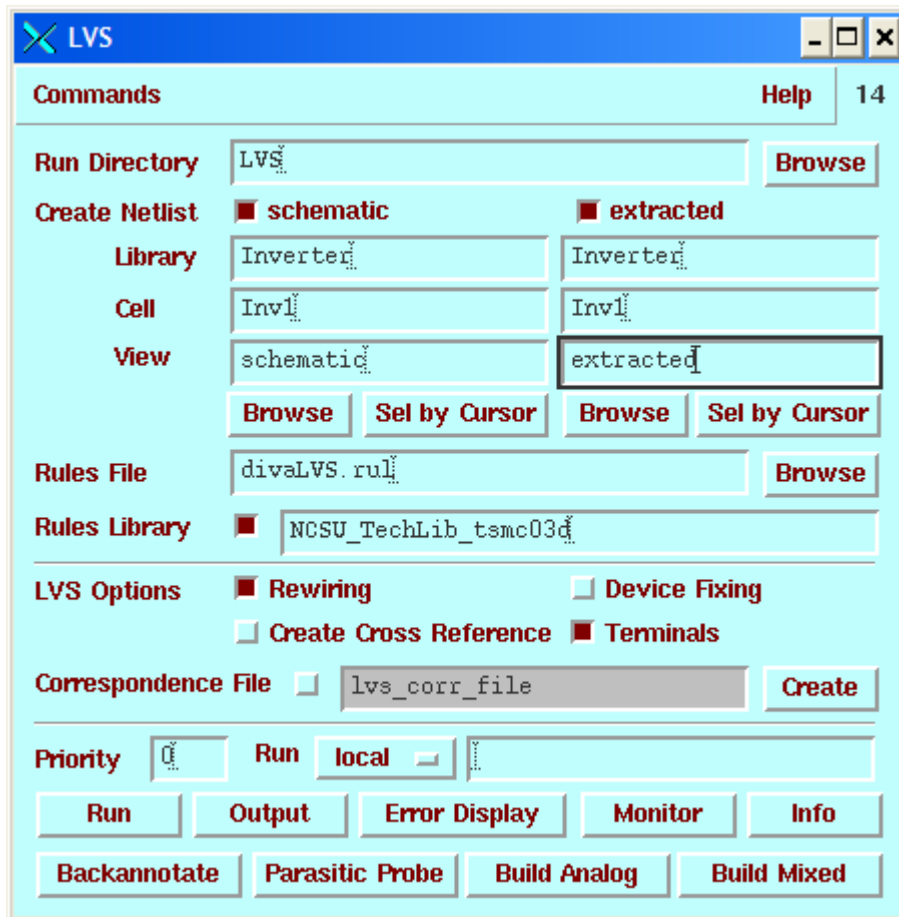
There will also be a new view in your cell called “extracted”. You don’t need to do anything with this view for now, but if you look at it you will notice that it looks a lot like your layout, but has transistor symbols on it indicating devices that the extractor found. You can zoom in on these devices and see what net names they are connected to and compare this to your schematic if there are any problems.

Making LVS Check FET Parameters

The default LVS settings do not check for size mismatch between transistors. To enable this, choose NCSU→Modify LVS Rules... from the layout editor and make sure the “Compare FET Parameters” checkbox is enabled.

Starting LVS

If there are no errors during extraction, choose Verify→LVS... from the layout editor and make sure all of the fields match those shown below.



Click “Run” to start the check. It will execute in the background and notify you a few seconds later when the check is complete. It will say that the LVS job failed or succeeded. This doesn’t refer to the verification result, but only whether it was able to even start the check. If it failed, “Check and Save” the schematic and try running LVS again. If that doesn’t work, make sure you entered the library and cell names correctly.

Once LVS succeeds, click the “Output” button to view a text file listing the results. It will have some summary information, such as a list of the number of devices and nets in each cell view. What you are looking for is a line that says “The net-lists match”.

```
/home/aa/grad/bsl/class/ee141/LAB3/LVS/si.out
File Help 16
[@(#) $CDS: LVS version 4.4.5 04/20/2000 16:37 (cds11182) $
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/aa/grad/bsl/class/ee141/LAB3/LVS/layout/netlist
count
4      nets
4      terminals
1      pmos
2      nmos

Net-list summary for /home/aa/grad/bsl/class/ee141/LAB3/LVS/schematic/netlist
count
4      nets
4      terminals
1      pmos
1      nmos

Terminal correspondence points
1      GND
2      VDD
3      VIN
4      VOUT

The net-lists match.
```

If instead you get “The net-lists match logically, but have mismatched parameters”, that means that both the schematic and layout have the same type of transistors hooked up the same way, but the device sizes don’t match. In this case, it would mean that the layout is still a standard inverter, but it won’t perform the same as the one in your schematic.

If the LVS check turns up errors, they will generally be listed twice. First it lists things in the schematic that it couldn’t find a match for in the layout, and then it lists things in the layout it couldn’t find a match for in the schematic. These errors will help you find the problem, but they can be very cryptic difficult to follow. As you become experienced with LVS checking, you will get some intuition about how to follow these errors, and learn some techniques to track them down somewhat systematically.

At some point you will find yourself with a layout that you think is “clean” but LVS reports errors. You will insist until you are blue in the face that the computer is wrong. Be assured that this is not the case. Sometimes the error is subtle or different from what is listed in the error report, but LVS doesn’t report errors if your cell is truly clean. You will be very mad at LVS until you find the problem, at which point you will be very happy that LVS was there for you.