BILL HUNG

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OBJECTIVE Full Time Position in August 2006

EDUCATION

B.S. Electrical Engineering and Computer Science Major — Graduating August 2006
University of California, Berkeley — Overall GPA 3.82 — Major GPA 3.77 (127 Semester Units)

EXPERIENCE

1. **Website Designer** — *Multiple Companies* — – Present
   Programmed in PHP, SQL, CGI, and HTML. Developed webpages for a college club, private company, and my project experience at http://career.billhung.net.
2. **Undergraduate Researcher** — *Tohoku University Nano-Spin Center, Japan* — – Spring 2005
   Tested a quantum computer using superconductor quantum theories. Handled superconductor at 0.04 Kelvin. Changed 100 liters of liquid helium and nitrogen gas. Submitted final report in IEEE LaTeX format.
3. **Exchange Student** — *Japan Engineering Program, Japan* — – Spring 2005
   Received a full scholarship. Presented verbal and written reports in Japanese. Achieved a 4.0 GPA in Japan.
4. **Research Assistant** — *Berkeley Sensor and Actuator Center, UC Berkeley* — – Fall 2004
   Developed the hardware and software of a portable Raman Medical Imaging System for Intel. The design, with the laser, was 15 times smaller than a commercial model.
5. **College Tutor** — *Internship at De Anza College* — – Year 2004
   College-level mathematics, physics, chemistry, and circuit analysis tutor. Mentored 5 under-achieving students to achieve academic success.
6. **President and Founder** — *Science and Engineering Association* — – Fall 2003
   Planed visits to Stanford Linear Accelerator Center (SLAC) and the Intel Museum. Organized seminars of successful engineers to speak to 100 members and 10 officers. Increased the funding from $100 to $1,000.

PROJECTS

1. **Static Random Access Memory (SRAM) Transistor Level Layout Design** – Spring 2006
   Designed the layouts with Cadence Virtuoso, completed the schematics, and simulated the SRAM with HSPICE.
2. **Peer-to-Peer Network Socket Programming (TCP, UDP, and IP)** – Fall 2005
   Constructed an Overlay Network with a HTML user interface. Low-Level UDP/IP Protocol with timing constraints.
3. **LCD Display, FPGA, and N64 Controller Interfacing using Verilog** – Fall 2005
   Created a game on an Xilinx FPGA board. Asynchronous interfacing with a N64 Controller. Handled multi-clock accessing of SDRAM. Output data to a 17-inch LCD screen.
4. **Network Broadcasting Digital Music Player on Field Programmable Gate Array (FPGA)** – Spring 2005
   Designed a circuit to transform music data from the network to the speaker connected to the FPGA board using Verilog. Interfaced with an audio AC 97 chip and the Ethernet network ports. Output to a text-based LCD.
5. **Mixed Signal DC Stepping Motor Driver Circuit** – Spring 2005
   Designed a Bipolar-CMOS circuit to control the rotation of a DC Stepping Motor. A synchronized digital circuit controlled a 5-Watt motor through 4 bi-polar amplifiers.
6. **Transistor Level CMOS Amplifier** – Fall 2004
   Designed an amplifier with 1000 times signal gain, 2 mV to 4 mV input voltage, and 34 mW power consumption.
7. **CPU Design using Hardware Description Language (HDL)** – Fall 2004
   Built a CPU using Verilog. Verified the CPU design with MIPS assembly instructions. Handled pipelining issues.
8. **Analog Audio Equalizer Op-Amp Circuit** – Summer 2004
   Built a circuit for a MP3 player. Optimized the output frequency range, output amplitude, and attenuation level.

COMPUTER SKILLS

Operating Systems: OSX (10.4 Tiger), Linux/Unix (Fedora, Solaris, Knoppix), Windows, MS-DOS
Programming: Verilog, C, C++, PHP, TCL, Java, HTML, XML, CGI, LaTeX, LabView, MIPS, SQL
Applications: SPICE, ModelSim, Cadence Virtuoso, Synplicity Synplify, ChipScope, Matlab, GCC/GDB

ACADEMIC AWARDS

JASSO Scholarship (Spring 2005)
Faculty Association Scholarship (Spring 2004)
Student Body 4.0 GPA Scholarship (Fall 2003)
Carlolee Erickson Inter Club Council Scholarship (Fall 2003)

OTHERS

Fluent in English, Japanese, and 3 dialects of Chinese (Mandarin, Cantonese, Hakka).