UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

# EECS150 Fall 2005 Project
## Electronic Etch-A-Sketch
## Final Project Report

## 1.0 Report Description

The final report is a technical description of the device that you have designed and built for your project.

The main purposes of documentation are:
1. Allow users to understand and operate your device.
2. Help your fellow engineers to understand your design so it can be upgraded, improved, and maintained.

Your goal should be to ensure that your design will be useful even if you are no longer around to explain its function. Without adequate documentation, many great designs are sent to the scrap heap.

For this semester, since the SDRAM controller and arbiter, the paint engine are the heart of the project, we want them to be given the most emphasis. Make sure to leave time for editing, typing, and proof-reading; nothing is more annoying than trying to read documentation that has obviously never been proof-read.

## 2.0 Report Outline

This is the closest you will get to detailed specification for the contents of your report. It is your job to design, write and edit your report as well as produce diagrams that will adequately document your design. Your report should closely follow the outline specified below.

**You report, excluding the cover page and table of contents may total no more than 10 pages of text and 20 pages with diagrams**. You may include diagrams within the text or on separate pages at the end. We suggest using Microsoft Visio for the diagrams; they are available on the lab computers. If you decide to (hand) draw your diagrams, be sure to use a ruler or graph paper, messy diagrams are useless.

1. Cover Page
2. Table of Contents
3. Abstract
   a. Approximately 1 paragraph
   b. Your abstract should be about your project
   c. Describe your design, not the project requirements
4. Overview (1-2 pages)
   a. Design (Block Diagram)

            i.   You may NOT use our diagrams
          ii.   You may draw this by hand, but use a ruler
        iii.   You must show more detail than our diagrams
        iv.   You diagram should be easily read and understood
    b.  Brief Description of Major Sub-Modules
            i.   Keep this part short
          ii.   Do not repeat the assignment specification
        iii.   Add details about how you changed or added to the assignment specifications

5.   System Description (5-6 pages)
    a.  Include detailed figures
            i.   You may NOT use our diagrams
          ii.   You may draw these by hand, but use a ruler
        iii.   You must show more detail than our diagrams
        iv.   You diagrams should be easily read and understood
    b.  Subsystem 1: N64 Controller
            i.   Short Section
          ii.   Block and Bubble-and-Arc diagrams
        iii.   Module decomposition / Block Diagram (if you have multiple modules)
        iv.   Serial transmission and capture description
    c.  Subsystem 2: Paint Engine
            i.   Include a detailed block diagram
          ii.   Modules
               1.   Block diagram showing connections
               2.   Show what state is in each module
               3.   Describe what each piece of state represents
        iii.   Theory of operation
               1.   How does it fit together
               2.   Bubble and Arc Diagram
    d.  Subsystem 3: SDRAM Control and Arbiter
            i.   SDRAM Arbiter
          ii.   Router (Static or Dynamic)
        iii.   Block and Bubble-and-Arc diagrams
    e.  Subsystem 4: Video/FIFO
            i.   Short Section
    f.  Design Tradeoffs
            i.   Did you have to sacrifice any features to make it work?
          ii.   What did you change as a result of debugging?
        iii.   What would you design differently next time?

6.   Design Metrics (1 page absolute max)
    a.  Number of 4LUTs
    b.  Design and debugging time estimates
            i.   Design Time
          ii.   Time for each checkpoint
        iii.   Time spent writing Verilog

                iv.  Debugging time
7.  References
      a.  Note any and all source files that are not your own
          i.  Give a description of its function
         ii.  May have to include diagrams if the code is crucial to your project and the code is complicated.
              1.  We know that fpga_top.v, register.v, and counter.v are ours and we know how they work. We don't need too much detail on these.
      b.  Cite where you obtained the code or idea.
         i.  WWW, book, etc.
         ii.  Ideas that other groups significantly contributed.
8.  Conclusion (1 page)
      a.  Summary of main features
      b.  Problems Encountered
      c.  What would you do differently next time
9.  Suggestions (1 paragraph)
      a.  What was too difficult
      b.  What should we do differently

For the overview section, try to give a "breadth before depth" introduction to your project. Your readers need to get a general picture of your system before they can understand the details. Describe the user visible features; save the detailed inner workings for the system description section. You should have a general block diagram in this section. Try not to duplicate our description of the assignment too much; we already know what we assigned you. Also, do NOT use our block diagrams, you will lose many points and besides your project won't completely match our diagrams.

The detailed system description can start with functional and input/output specifications. Modules can be described in order from input to output, or from most to least important module. Illustrate the descriptions with the block diagrams and timing diagrams you have prepared; refer to these as figures. Don't bother going into the details of very simple modules, especially the ones we provide you. However, do give detailed descriptions and figures for your SDRAM Controller, Arbiter and FIFO interface as well as your game engine and everything in it.

For the conclusion, summarize the key design features. What will the reader need to be careful about if they were to attempt to duplicate or modify your design? And, what are possible improvements which could be made to the design?

# 3.0 Hints

1.  Type this report. DO NOT hand write it
      a.  Diagrams and figures are an exception. Visio is preferred, but if you are going the hand-drawn route, please make them neat by using a ruler and/or graph paper.
2.  Use standard 8.5 by 11 paper throughout the report.
      a.  Diagram pages may be on larger sheets.

       b.  Larger sheets for diagrams are easier to follow, and can be neatly folded to fit in a standard binder.

3.  Minimum 12pt font, single spaced with 1 inch margins.
4.  Page Limit
       a.  Cover page and Table of Contents are not included in the page limit
       b.  Text portion of report should not exceed 10 pages.
       c.  Appendices, including timing diagrams and schematics can be up to 20 pages MAXIMUM.
       d.  Anything after 20 pages will be torn off and IGNORED.
5.  Make a copy of your report for safety.
6.  Make sure the copy you hand in is easily readable.
7.  Include block diagrams, bubble and arc diagrams, timing diagrams, state diagrams, and tables as appropriate and on or as near as possible to the page in which they are referenced.
       a.  Do NOT include any Verilog in your report.
8.  Put titles on all figures and diagrams.
9.  Put some thought into this
       a.  Poor documentation will degrade the perceived quality of your work
       **b.  This report is worth as much as a checkpoint**

## 4.0 Submission

Reports are due Wednesday 12/7 at 10am.
**DO NOT HAND IN PRINTED VERILOG**.

Please submit an electronic copy to "U:\Project Submission Directory", the same folder that you submitted your project. The electronic copy need not be complete; it may be missing diagrams and anything else hand-drawn.

We will primarily base your grade on the paper copy of your report you will submit to the homework box by 10am on 12/7. We will not accept any reports after 10:10am, no exceptions.

You and your partner should also separately fill out a partner evaluation. There are two copies of the partner evaluation at the end of this document. Your partner eval is also due at 10am.

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# EECS150 Fall 2005 Project
## Electronic Etch-A-Sketch
## Partner Evaluation
## Submitted 12/7/2005

|  | Last Name | First Name | Login | SID |
|---|---|---|---|---|
| You |  |  |  |  |
| Partner |  |  |  |  |
| Lab Section |  |  |  |  |

Please indicate the percentage of work both you and your partner did.  **You and your partner must BOTH submit a copy of this form.**

If you partner did not put in their fair share of work, this is your last chance to tell us.  We will investigate the matter if you **check the line below.**
Please be honest.

Percentage of work done by partner:                                      _____

I felt that this was unfair:                                                   _____

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I felt that this was unfair:                                                      _____