University of California
College of Engineering
Department of Electrical Engineering and Computer Sciences

	Problem Set 7	**EE40**
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Reading:

Chap 7-7.5 of Hambley.
Chap 5.1-5.3.2, 5.4-5.4.2, 5.5-5.5.2 of Rabaey

Problems:

Chap 7: 7.5, 7.8, 7.22, 7.23, 7.28, 7.29, 7.32, 7.35-37 (sum-of-products only), 7.42, 7.52, 7.55, 7.56

Additional Problems:

Problem 1
Let $F = \bar{a}bc + a\bar{b}c + ab\bar{c} + abc$

(a) Set up the truth table for F.

(b) Use K- maps to minimize F.

(c) Using only NAND gates, implement the logic function $G = a\bar{b}\bar{c}$ + c

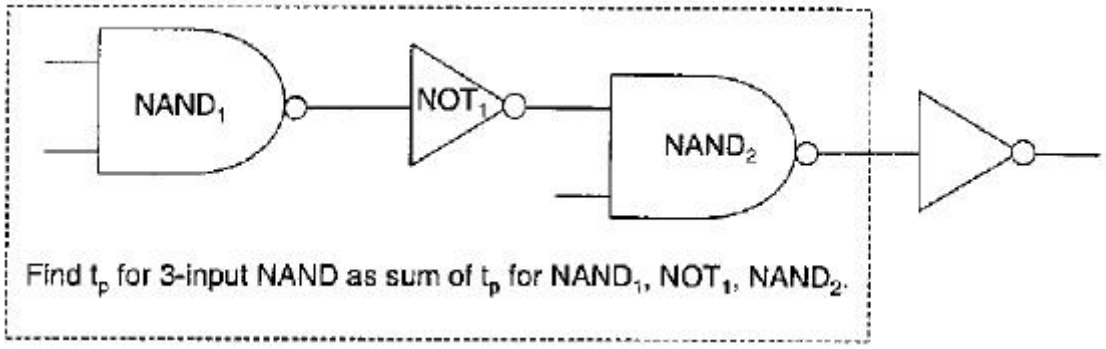
Problem 2
Consider a CMOS inverter gate composed of transistors with $R_{eq,NMOS}$ = 1 kΩ an $R_{eq,PMOS}$ = 2 kΩ. Used the resistive switch model for the transistors.

(a) Find the propagation delay for a low-to-high transition assuming a load capacitance of 20 fF.

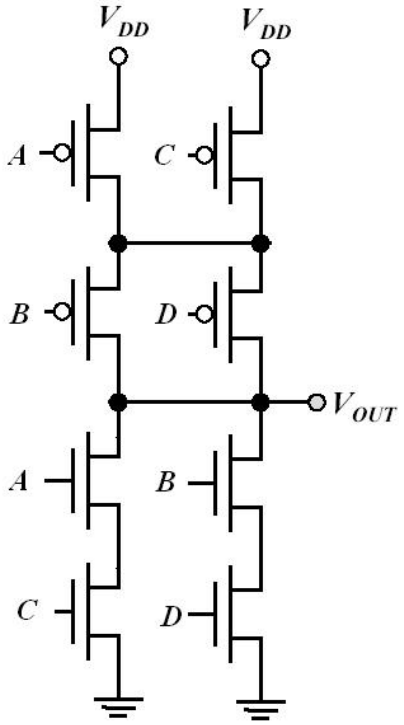
(b) Find the propagation delay for a high-to-low transition assuming a load capacitance of 20 fF.

(c) Assuming 1 input is tied to ground and the other is a square wave at 500 kHz, find the dynamic power dissipation.

Problem 3
Find the worst-case propagation delay for a 3-input NAND gate with inverter load, where the 3-input NAND is implemented from two 2-input NAND gates and an inverter as shown. Use $R_{eq,PDN}$ = 1 kΩ an $R_{eq,PUN}$ = 2 kΩ, and C_G = 10 fF per transistor.



Problem 4
Consider the following CMOS circuit:



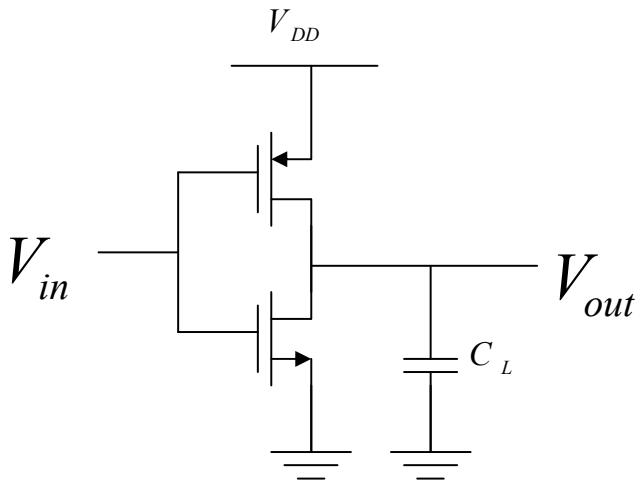
(a) Write the sum-of-products form of the logic function implemented.

(b) Draw an implementation of this using only NAND gates.

(c) How many NAND gates did you use? How many transistors is this? Compare this to the number of transistors used in the implementation shown above.

Problem 5

Consider the CMOS inverter shown below.



$V_{DD} = 2.5\,\text{V}$

$\mu_n C_{ox} = 3\mu_p C_{ox} = 100\,\frac{\mu A}{V^2}$

$(\frac{W}{L})_n = 10$

$V_{Tn} = -V_{Tp} = 1\ \text{V}$

$C_L = 10\,fF$

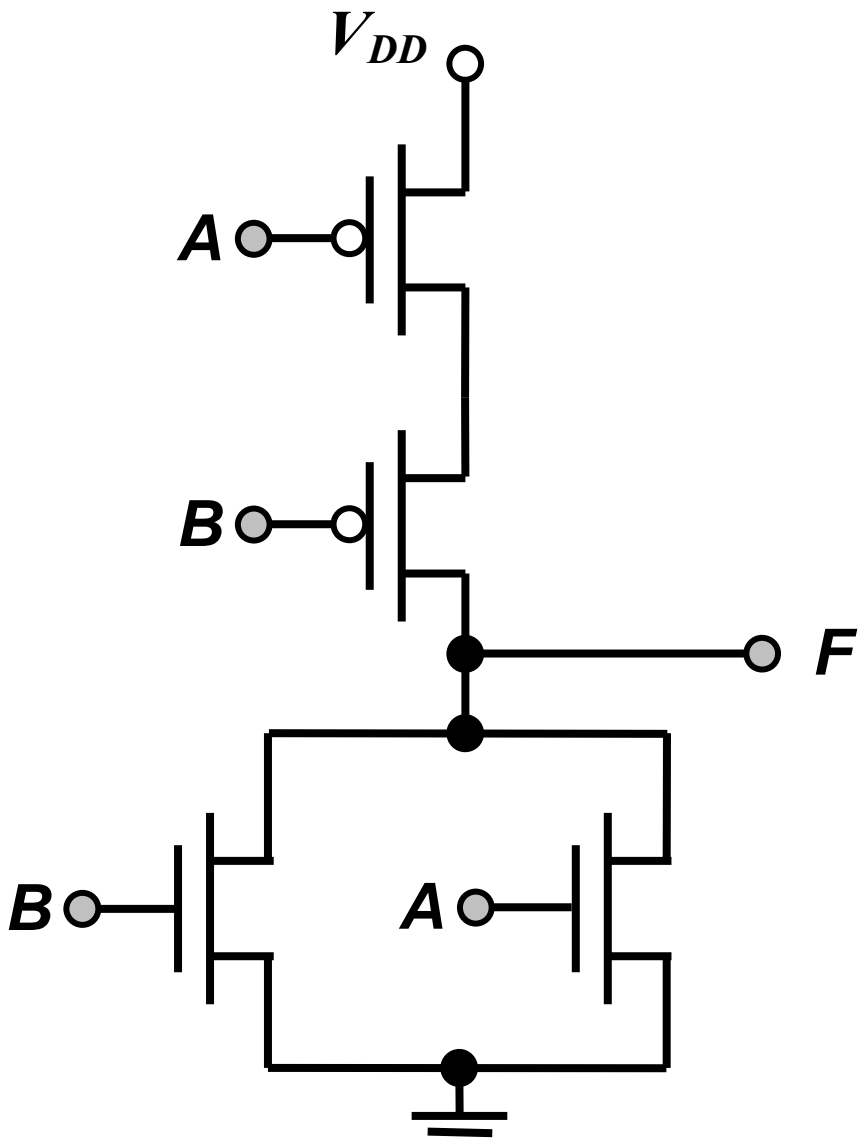
(a) What is the value of V_{in} and V_{out} to make I_{Dn} maximum?

(b) What is the value of V_{in} and V_{out} to make $|I_{Dp}|$ maximum?

(c) Adjust $(\frac{W}{L})_p$ such that $t_{pLH} = t_{pHL}$.

(d) Assuming that the PMOS has the size that you found in part (c), find the propagation delay for this inverter.

Problem 6



Consider a CMOS NOR with $(W/L)_n = 1$.

(a) Find the $(W/L)_p$ such that $T_{PHL}=T_{PLH}$ when only one signal is changing at a time.
(b) Find the $(W/L)_p$ such that $T_{PHL}=T_{PLH}$ when only both signals are changing at a time.
(c) Redo the same exercise with a NAND gate.
(d) Why would someone prefer NAND gates over NOR gates.