EE40
HW 7 solution p1

P7.5 (a) $101.101 = 4+1+0.5+0.125 = 5.625$

(b) $0111.11 = 4+2+1+0.5+0.25 = 7.75$

(c) $1010.01 = 8+2+0.25 = 10.25$

(d) $111.111 = 4+2+1+0.5+0.25+0.125 = 7.875$

(e) $1000.0101 = 8+0.25+0.0625 = 8.3125$

(f) $10101.011 = 16+4+1+0.25+0.125 = 21.375$

P7.8 (a) $173 = 128+55$
$+32+23$
$+16+7$
$+4+2+1$
$= 10110111_2$
$= 0267$
$= 0xB7$

(b) $299.5 = 256+43.5$
$+32+11.5$
$+8+2+1+0.5$
$= 100101011.1_2$
$= 0453.4$
$= 0x12B.8$

(c) $735.75 = 512+223.75$
$+128+95.75$
$+64+31.75$
$+16+8+4+2+1+0.5+0.125$
$= 1011011111.11_2$
$= 01337.6$
$= 0x2DF.C$

(d) $313.0625 = 256+57.0625$
$+32+25.0625$
$+16+8+1+0.0625$
$= 100111001.0001_2$
$= 0471.08$
$= 0x139.1$

EE40 HW7 p2

(e) $112.25 = 64 + 48.25$

$+32 + 16 + 0.25$

$= 1110000.01_2$

$= 0160.2$

$= 0x70.4$

P7.22

(a)

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(b)

A	B	C	D	E
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(c)

W	X	Y	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

EE40 Hw 7 p3

(d)

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(e)

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

P7.23

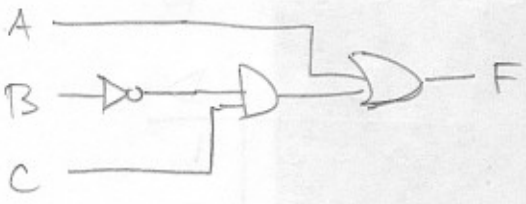
(a) $F=(A+B)\overline{C}$

(b) $F = (A+B) + \overline{BC}$

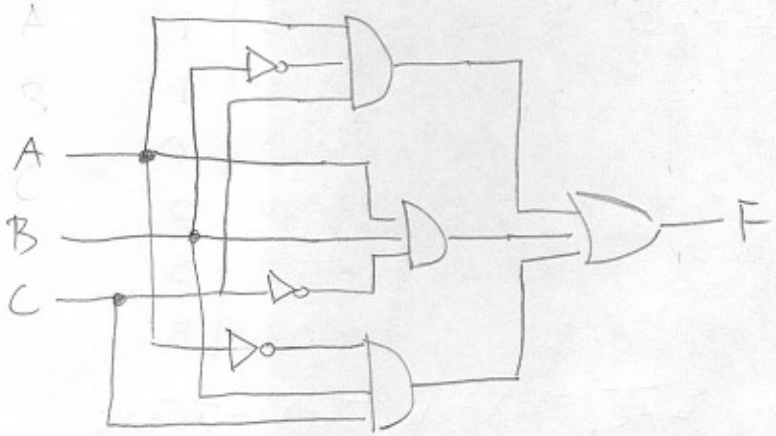
(c) $F = D + AB + \overline{BC}$

P7.28

(a)



(b)



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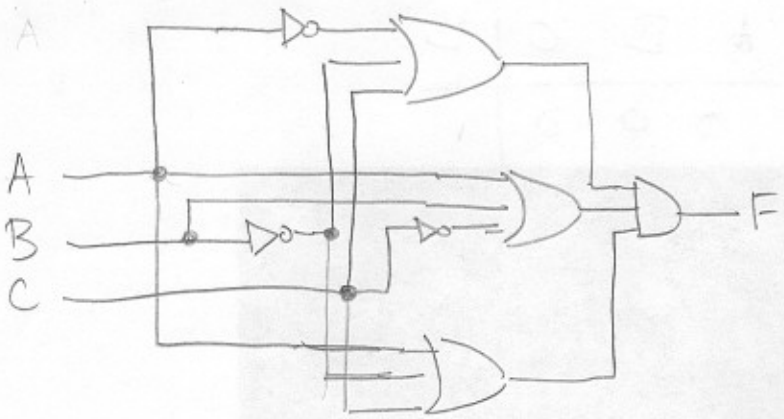
(c)



P7.29

(a) $F = \overline{(\overline{AB})(\overline{(\overline{C}+A)\overline{D}})} = \overline{(\overline{A}+\overline{B})(\overline{(\overline{C}+A)}+D)} = \overline{(\overline{A}+\overline{B})(C\overline{A}+D)}$

(b) $F = \overline{\overline{(A(\overline{B}+C))}\,\overline{D}} = \overline{(A+(\overline{B}+C))\overline{D}} = \overline{(A+B\overline{C})\overline{D}}$

(c) $F = \overline{(A\overline{B}C)(\overline{A(B+C)})} = \overline{(\overline{A}+B+\overline{C})(A+\overline{(B+C)})} = \overline{(\overline{A}+B+\overline{C})(A+\overline{B}\overline{C})}$

(d) $F = \overline{\overline{(A+B+C)}+\overline{(A+\overline{B}+C)}+\overline{(\overline{A}+B+\overline{C})}} = \overline{A\overline{B}\overline{C}+\overline{A}BC+A\overline{B}C}$

(e) $F = \overline{(\overline{ABC})(\overline{A\overline{B}C})(\overline{\overline{A}B\overline{C}})} = \overline{(\overline{A}+\overline{B}+\overline{C})(\overline{A}+B+\overline{C})(A+\overline{B}+C)}$

P7.32

D is 5V when neither set of switches tie it to ground. That is, $D = \overline{(A+\overline{B}C)}$

$= \overline{A}(B+\overline{C})$

$= \overline{A}B+\overline{A}\overline{C}$

A	B	C	D
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

P7.35 $F = \overline{A}\overline{B}\overline{C}+\overline{A}B\overline{C}+A\overline{B}C+ABC = \overline{A}\overline{C}(\overline{B}+B)+AC(\overline{B}+B) = \overline{A}\overline{C}+AC$

P7.36 $F = \overline{A}\overline{B}\overline{C}+\overline{A}BC$

P7.37 $F = \overline{\overline{A}BC} = A+\overline{B}+\overline{C}$

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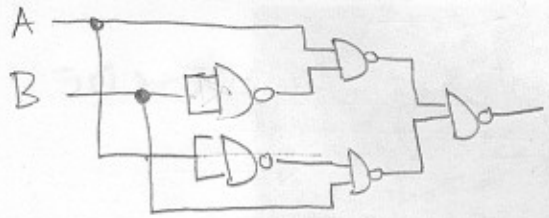
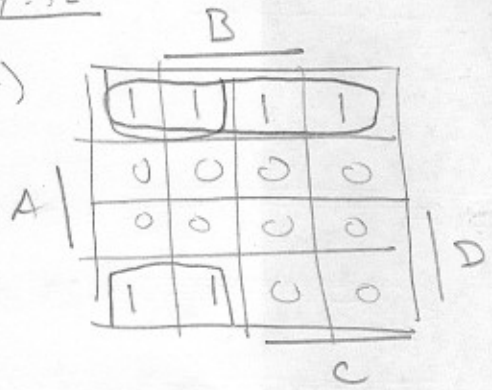
P 7.42

$$A \oplus B = A\bar{B} + \bar{A}B = \overline{(\overline{A\bar{B}})(\overline{\bar{A}B})}$$



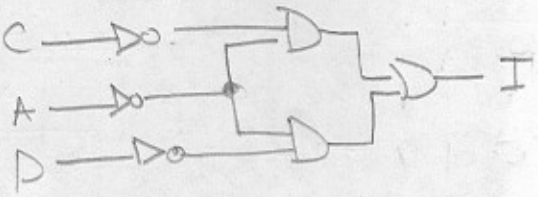
P 7.52

(a)

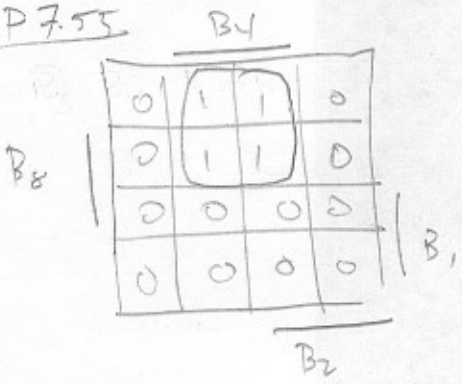


(b) $I = \bar{A}\bar{D} + \bar{A}\bar{C}$

(c)

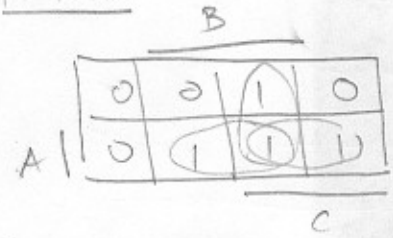


P 7.55



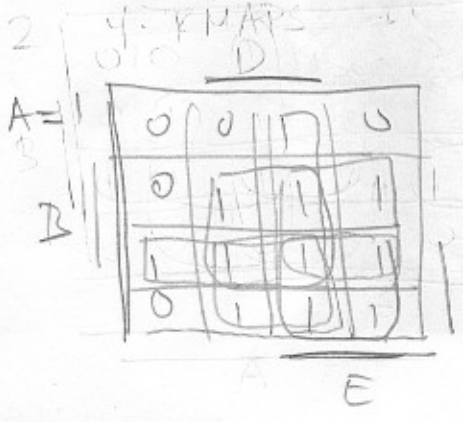
$F = \overline{B_1} B_4$

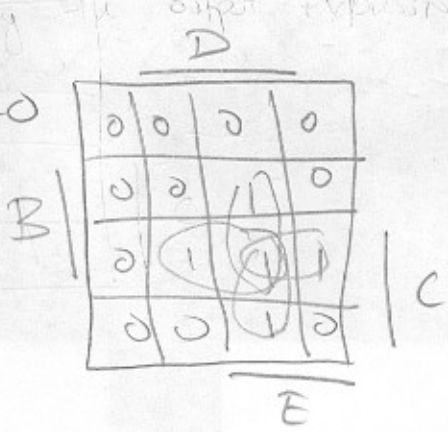
P 7.56



$X = AB + AC + BC$

A. 5-KMAP is 2 4-KMAPS layered on top of one another.





EE to HW7p6

Notice that each of the 2-cubes in the A=0 Map extend through to the A=1 map so we can supress the $\bar{A}$ part of each min-term.

$$X = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$$

Problem 1

(a)

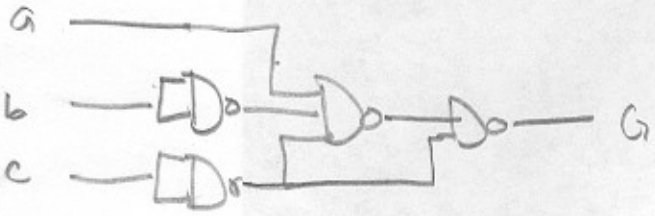
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b)

A \ B	0	0	1	0
0	0	1	1	0
1	0	1	1	1

C

(c) $G = a\bar{b}\bar{c} + c = \overline{\overline{(a\bar{b}\bar{c})}(\bar{c})}$



Problem 2

(a) $\tau_{PLH} = \ln 2 \; R_p C_L = (\ln 2)(2k\Omega)(2fF) = 27.73\ ps$

(b) $\tau_{PHL} = \ln 2 \; R_n C_L = 13.86\ ps$

(c) Const. input → no dynamic power dissipation.

Square wave: $P_{dyn} = C_L V_{DD}^2 f = (2fF)(5V)^2(500kHz) = 250\ nW$

Problem 3

Because the resistance for the pull-up network is higher, the worst case is a low-to-high transition.

For the 1st NAND gate:

$\tau_{pLH} = \ln 2 \, R_{PUN} C_L$ where $C_L = 2C_G$ since the output goes to 2 transistors in the inverter

$= (\ln 2)(2k\Omega)(2\,aF) = 27.73\,ps$

If the NAND gate is making a low-to-high transition, the NOT must be making a high-to-low

$\tau_{pHL} = \ln 2 \, R_{PDN} C_L$ where $C_L = 2C_G$

$= (\ln 2)(1k\Omega)(2aF) = 13.86\,ps$

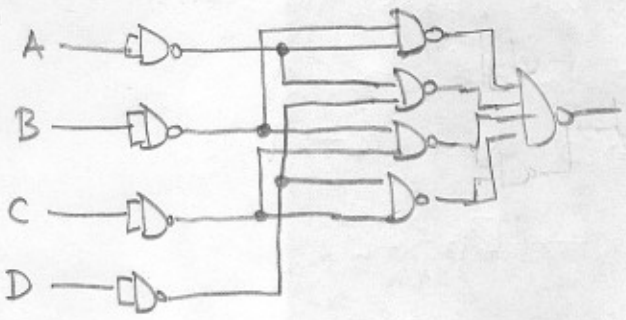
The second NAND will be just like the first NAND (leaving the second input at V_{DD} and transitioning the other to zero results in a low-to-high transition

$\tau_{total} = 2(27.73ps) + 13.86ps = 69.3\,ps.$

Problem 4

(a) $V_{OUT} = (\bar{A}+\bar{C})(\bar{B}+\bar{D}) = \bar{A}\bar{B} + \bar{A}\bar{D} + \bar{B}\bar{C} + \bar{C}\bar{D}$

(b)



(c) 9 including a 4-input NAND. (You could have had various other ways of doing this)

Here I have 40 transistors which is much more than 8.

EE 466 HW 7 P8

Problem 1

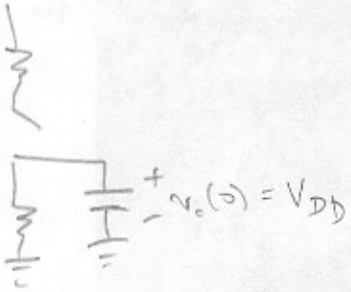
(a) If we assume the input cannot change faster than the time constant, we can think of the capacitor as an open circuit. In that case, the maximum current occurs when both transistors are in saturation.

Assuming $\left(\frac{W}{L}\right)_p$ is chosen so $\tau_{PLH} = \tau_{PHL}$ or $k_n = k_p$

$$I_{Dn} = \frac{1}{2}k_n(V_{in} - V_{Tn})^2 = \frac{1}{2}k_p(V_{DD} - V_{in} - V_{Tp})^2$$

$V_{in} = V_{in} = \frac{V_{DD}}{2}$, $V_{out} = \frac{V_{DD}}{2}$ [This is full credit]

However, if we assume the input can change very fast, we get max current on a high-to-low transition



$$I_{Dn} = \frac{v_c}{R_n}$$

$I_{Dn\,max}$ occurs when v_c is the highest (initially)

This is $V_{in} = 0 \to 1$ $V_{out} = 1 \to 0$

(b) This would be the same if we used the first method, but for the second it would be

$V_{in} = 1 \to 0$ $V_{out} = 0 \to 1$

(c) $\tau_{PLH} = \ln 2 R_p C_L$ $\tau_{PLH} = \tau_{PLH} \to R_p = R_n$

$\tau_{PHL} = \ln 2 R_n C_L$

$$\to \frac{3}{4}\frac{V_{DD}}{I_{SAT\,n}} = \frac{3}{4}\frac{V_{DD}}{I_{SAT\,p}}$$

$$\to I_{SAT\,n} = I_{SAT\,p}$$

$$\to \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}_n\right)(V_{DD} - V_{Tn})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p(-V_{DD} - V_{Tp})^2$$

Plugging in and solving gives us: $\left(\frac{W}{L}_p\right) = 30$

HW7 solu p9

(d) $\tau_p = \ln 2 R_n C_L \ln 2 \frac{3}{4} \frac{V_{DD}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{DD}-V_{Tn})^2} C_L = 1.155 \times 10^{-10}$ s

Problem 6

(a) Using the values from the previous problem... $\mu_p C_{ox} = \frac{1}{3}\mu_n C_{ox}$

$\tau_{PLH} = 2 R_p C_L$

$\tau_{PHL} = \frac{1}{2} R_n C_L \rightarrow \left(\frac{W}{L}\right)_p = 2 \cdot 3 = 6$

(b) $\tau_{PLH} = 2 R_p C_L$

$\tau_{PHL} = \frac{1}{2} R_n C_L \rightarrow \left(\frac{W}{L}\right)_p = 4 \cdot 3 = 12$

(c) For 1 signal:

$\tau_{PLH} = \frac{1}{2} R_p C_L$

$\tau_{PHL} = R_n C_L \rightarrow \left(\frac{W}{L}\right)_p = \frac{1}{2} \cdot 3 = \frac{3}{2}$

For 2 signals:

$\tau_{PLH} = \frac{1}{2} R_p C_L$

$\tau_{PHL} = 2 R_n C_L \rightarrow \left(\frac{W}{L}\right)_p = \frac{1}{4} \cdot 3 = \frac{3}{4}$

(d) We can get smaller designs with NAND gates