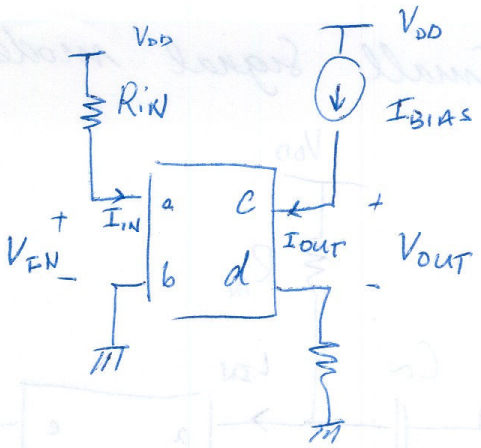
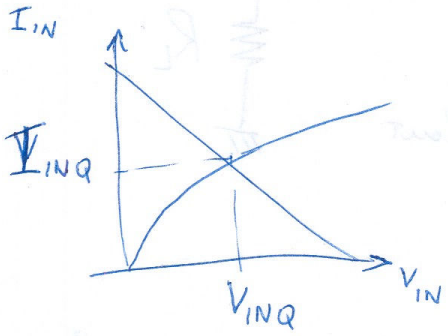
DC analysis:



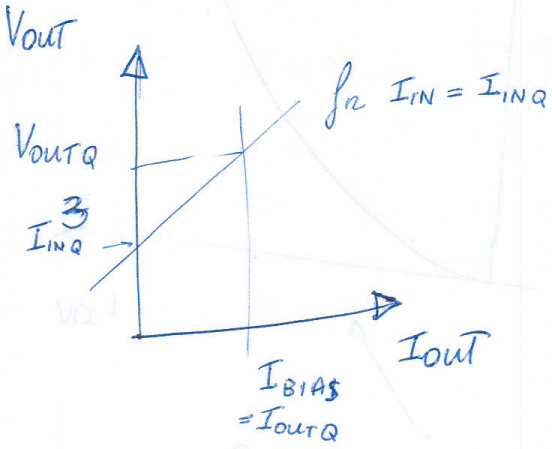
DC Bias Pt:

input load line

$$V_{IN} = V_{DD} - I_{IN} \cdot R_{IN}$$



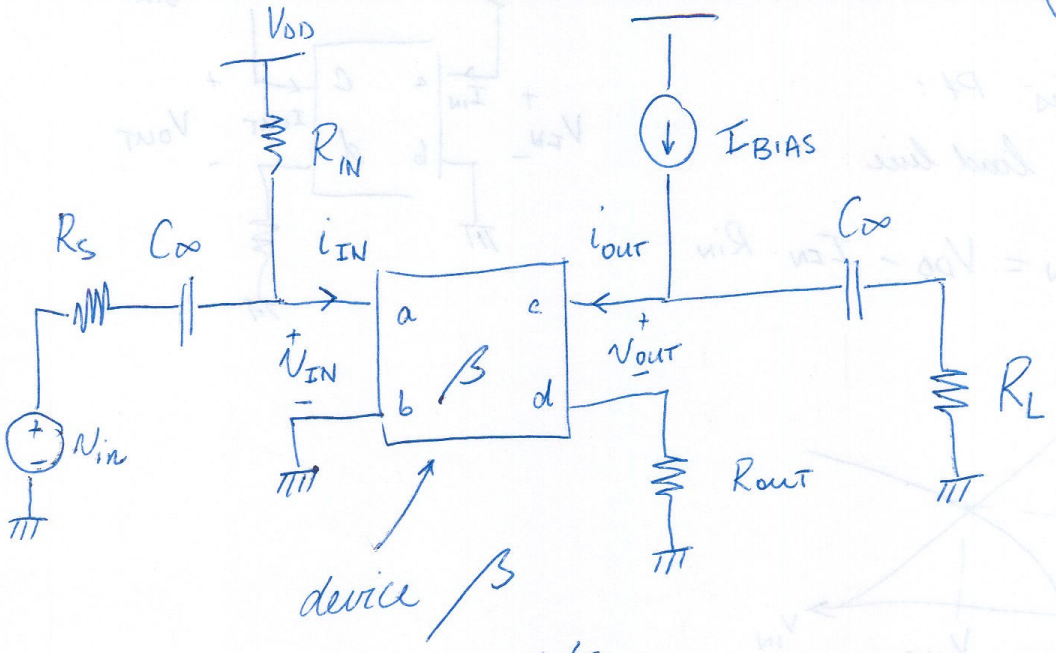
output Bias pt:



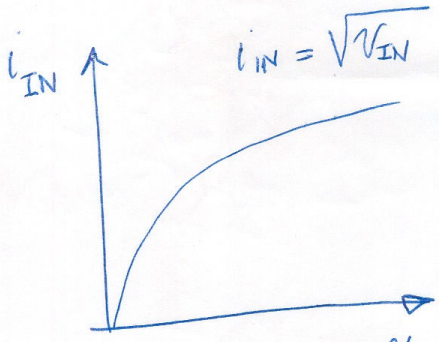
So we have I_{INQ}, V_{INQ}, I_{OUTQ}, V_{OUTQ}.

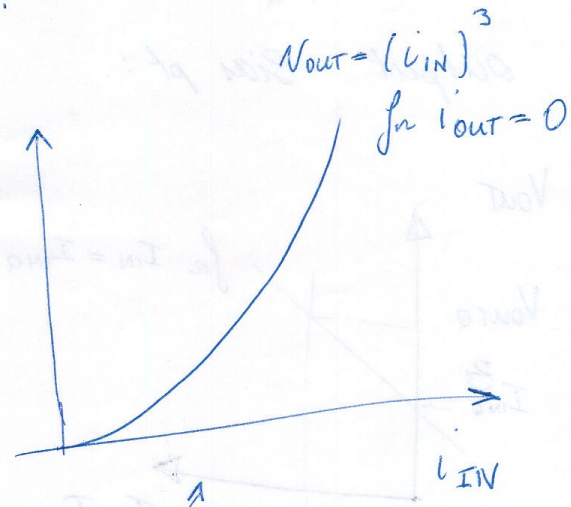
let's construct a SSM.

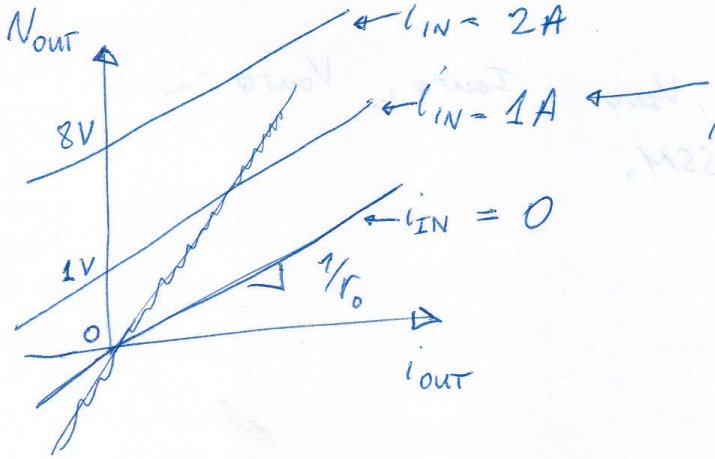
Small Signal model example:



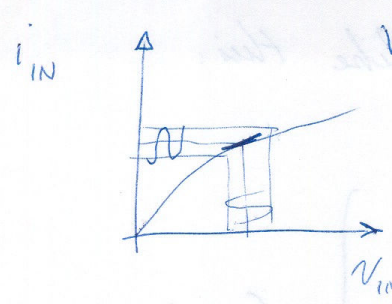
Device β characteristics:







$$V_{OUT} = (i_{IN})^3 + r_o\, i_{OUT}$$



$$i_{in} = \frac{\partial i_{IN}}{\partial v_{IN}}\bigg|_{V_{INQ},\, I_{INQ}} \cdot v_{in}$$

$$\Rightarrow \frac{\partial\left(\sqrt{v_{IN}}\right)}{\partial v_{in}} = \frac{1}{2}\frac{1}{\sqrt{v_{IN}}}\bigg|_{V_{INQ}}$$

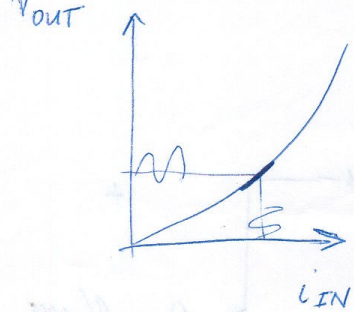
We can model:

$$r_{in} = \frac{2\sqrt{V_{INQ}}}{}$$

$$\Rightarrow i_{in} = \frac{1}{2}\frac{1}{\sqrt{V_{INQ}}} \cdot v_{in}$$

around V_{INQ}

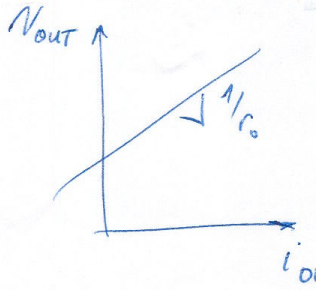
$$\Rightarrow v_{in} = r_{in} \cdot i_{in}$$



$$v_{out} = \frac{\partial v_{OUT}}{\partial i_{IN}}\bigg|_{I_{INQ},\, V_{OUTQ}} \cdot i_{IN}$$

$$\frac{\partial v_{OUT}}{\partial i_{IN}} = 3\, i_{IN}^{2}\bigg|_{I_{INQ}}$$

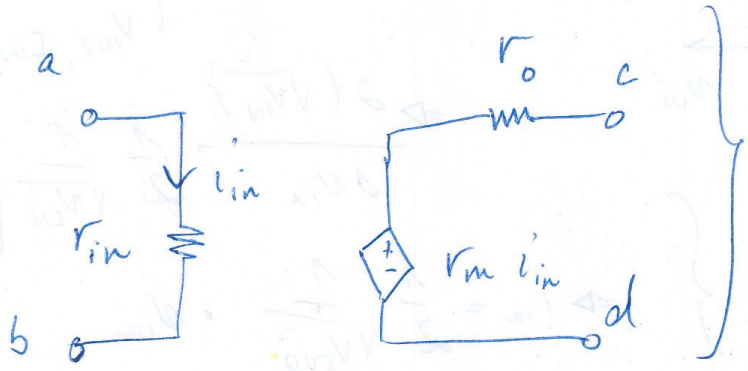
$$\Rightarrow v_{out} = \underbrace{3 \cdot I_{INQ}^{2}}_{r_m} \cdot i_{in}$$



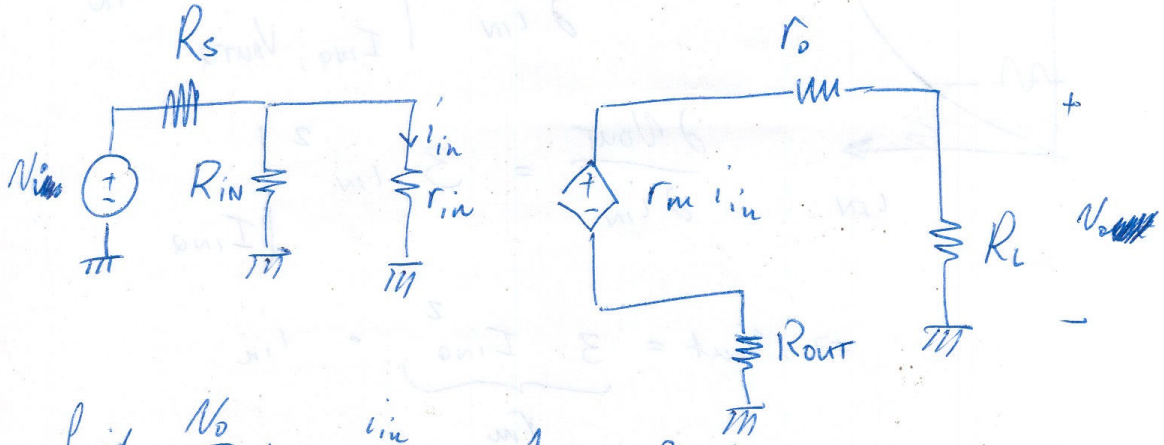
$$v_{out} = \frac{\partial v_{OUT}}{\partial i_{out}}\bigg|_{Q_{pt}} \cdot i_{out}$$

$$\Rightarrow v_{out} = r_o \cdot i_{out}$$

So the total model looks like this:



SSM of entire CKT:



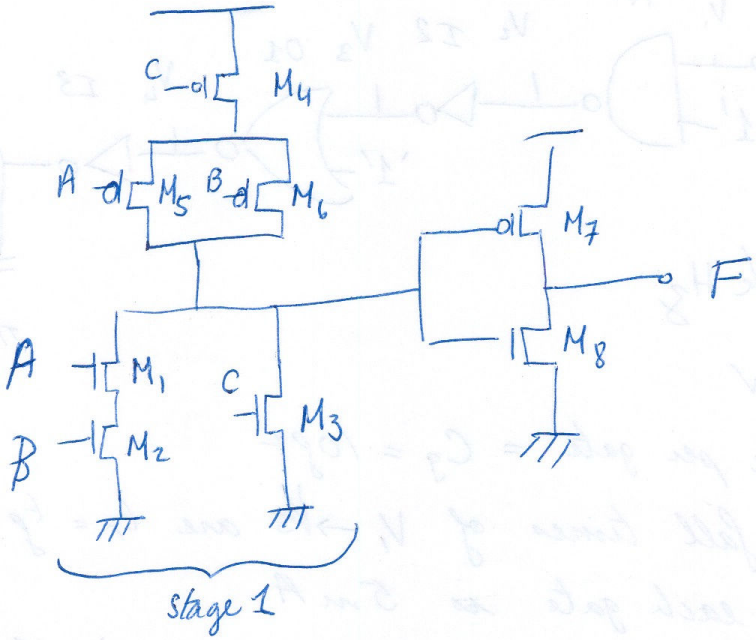
$$\text{Find } \frac{V_o}{V_i}: \quad \frac{i_{in}}{V_i} = \frac{1}{r_{in}} \cdot \frac{R_{IN} \| r_{in}}{R_{IN} \| r_{in} + R_S}$$

$$\frac{V_o}{i_{in}} = \frac{r_m \cdot R_L}{R_L + R_{out} + r_o}$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{1}{r_{in}} \cdot \frac{R_{IN} \| r_{in}}{R_{IN} \| r_{in} + R_S} \cdot \frac{r_m \cdot R_L}{R_L \cdot R_{OUT} + r_o}$$

CMOS logic

a) Implement $F = A \cdot B + C$ using transistors



b) $\mu_n = 3\mu_p$

Suppose $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2\left(\frac{W}{L}\right)_3$

and $\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 = 2\left(\frac{W}{L}\right)_1$

find t_{PHL}/t_{PLH} of stage 1 when

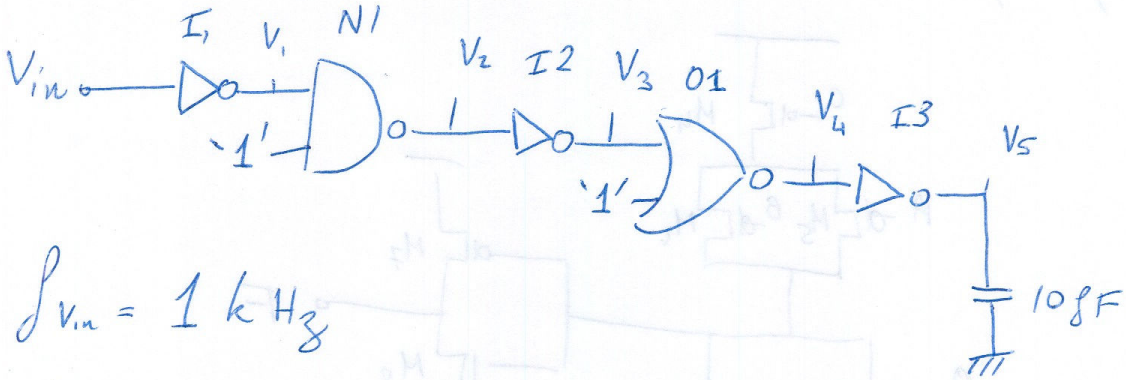
ABC goes from 100 → 111 and back.

PDN $\left(\frac{W}{L}\right)_{eq} =$ [illegible] $\left(\frac{W}{L}\right)_3 \times 2$

PUN $\left(\frac{W}{L}\right)_{eq} = \frac{1}{2}\left(\frac{W}{L}\right)_4 =$ [illegible] $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 \times 2$

But $\mu_p = \frac{1}{3}\mu_n \Rightarrow \frac{t_{PHL}}{t_{PLH}} = \frac{1}{3}$

CMOS Power Dissipation:



$f_{V_{in}} = 1\,kHz$

$V_{DD} = 5V$

Capacitance per gate $= C_g = 10fF$

Rise and fall times of $V_1 \rightarrow V_5$ are $t_r = t_f = 10ps$

I_{sc} for each gate is $5mA$

$I_{leakage}$ for each path to ground is $1nA$.

Find the total power consumption of this Design:

Dynamic power:

① Do not include power needed to charge V_{in} since this will be accounted for in the block driving this one.

② only V_1, V_2, V_3 toggle $\Rightarrow C_{eff} = 3 \times 2 \times 10\,fF = 60fF$

③ $P_{dyn} = C_{eff} \cdot V_{DD}^2 \cdot f_{V_{in}}$

Short-Circuit Power:

$E_{sc} = 3 \cdot V_{DD} \cdot I_{sc} \cdot t_r \Rightarrow P_{sc} = 3 \cdot V_{DD} \cdot I_{sc} \cdot t_r \cdot f_{V_{in}}$

↑ only 3 gates switch.

Leakage Power.

$P = 5 \cdot I_{leakage} \cdot V_{DD}$.

↑ since all 5 gates leak.