



Lecture #13

OUTLINE

- MOSFET I_D vs. V_{GS} characteristic
- Circuit models for the MOSFET
 - resistive switch model
 - small-signal model

Reading

- Hambley: Chapter 12.1-12.6
- Rabaey: Section 3.3

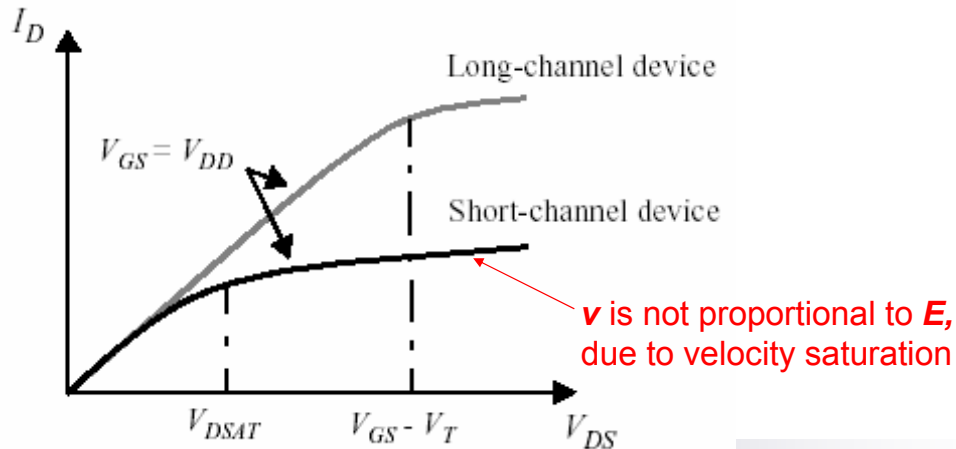


Velocity Saturation

At high electric fields, the average velocity of carriers is NOT proportional to the field; it saturates at $\sim 10^7$ cm/sec for both electrons and holes:

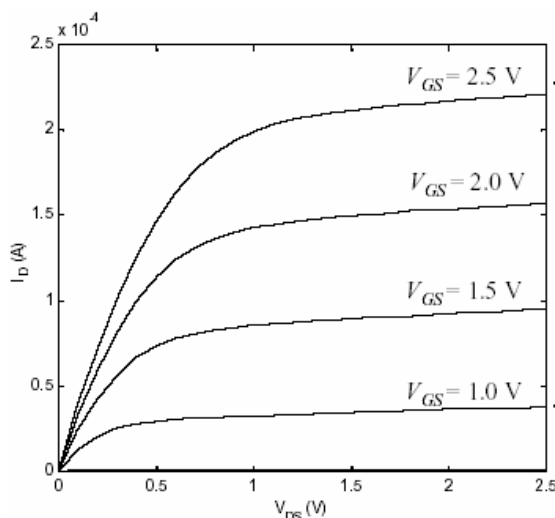
Current Saturation in Modern MOSFETs

- In digital ICs, we typically use transistors with the shortest possible gate-length for high-speed operation.
- In a very short-channel MOSFET, I_D saturates because the carrier velocity is limited to $\sim 10^7$ cm/sec



Consequences of Velocity Saturation

1. I_D is lower than that predicted by the mobility model
2. I_D increases linearly with $V_{GS} - V_T$ rather than quadratically in the saturation region

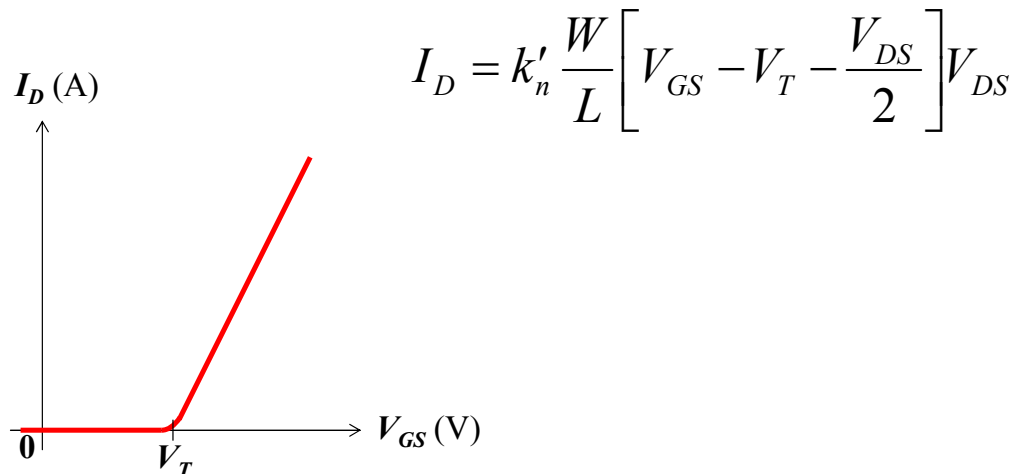


$$I_{DSAT} = WC_{ox} \left[V_{GS} - V_T - \frac{V_{DSAT}}{2} \right] v_{sat}$$

$$\text{where } V_{DSAT} = \frac{L}{\mu_n} v_{sat}$$

MOSFET V_T Measurement

- V_T can be determined by plotting I_D vs. V_{GS} , using a low value of V_{DS} :



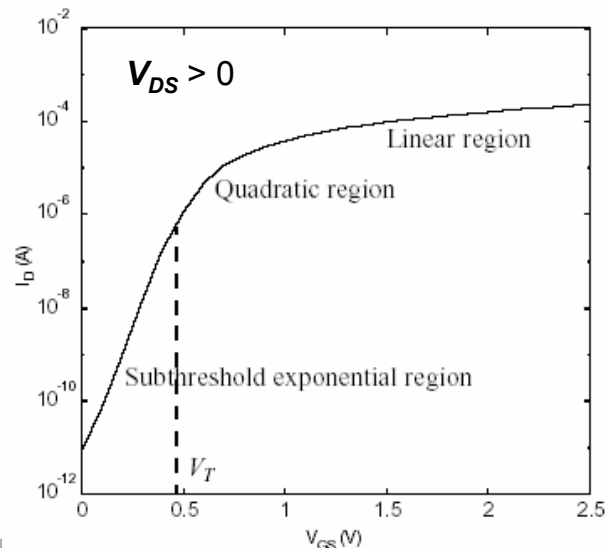
Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when I_D is plotted on a logarithmic scale:

- In the subthreshold ($V_{GS} < V_T$) region,

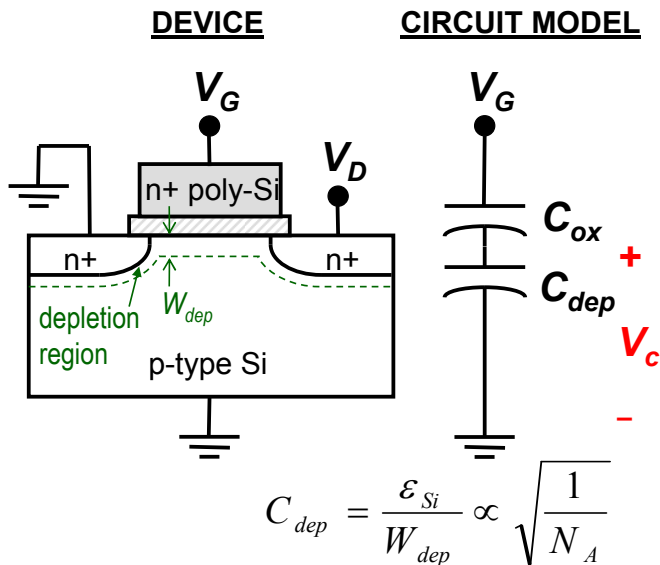
$$I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$$

This is essentially the channel-source pn junction current. (Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)



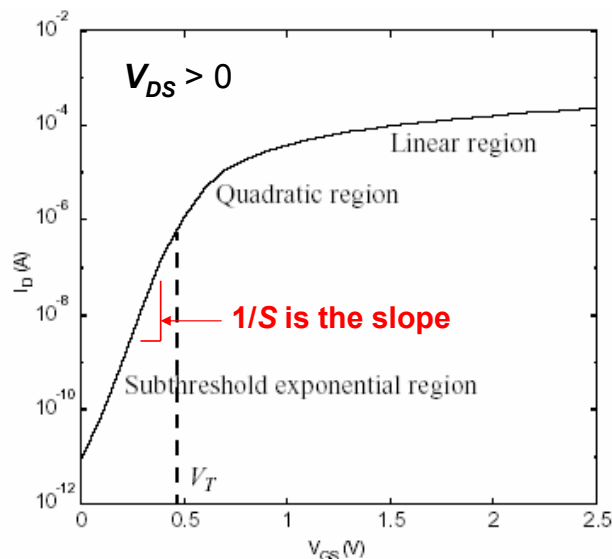
Qualitative Explanation for Subthreshold Leakage

- The channel V_c (at the Si surface) is capacitively coupled to the gate voltage V_G :



Slope Factor (or Subthreshold Swing) S

- S is defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region:



$$S \equiv n \left(\frac{kT}{q} \right) \ln(10)$$

Units: Volts per decade

Note that $S \geq 60$ mV/dec at room temperature:

$$\left(\frac{kT}{q} \right) \ln(10) = 60 \text{ mV}$$

V_T Design Trade-Off

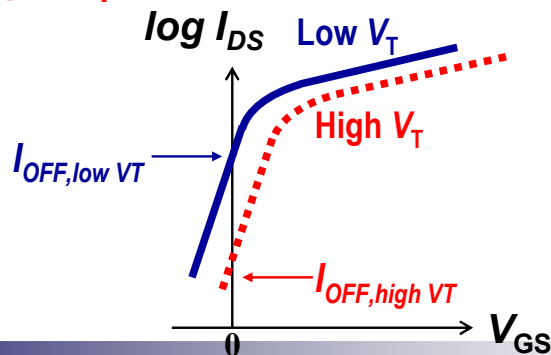
(Important consideration for digital-circuit applications)

- Low V_T is desirable for high ON current

$$I_{DSAT} \propto (V_{DD} - V_T)^\eta \quad 1 < \eta < 2$$

where V_{DD} is the power-supply voltage

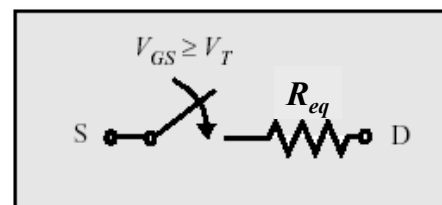
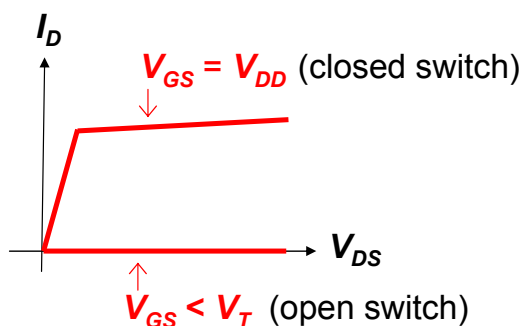
...but high V_T is needed for low OFF current



The MOSFET as a Resistive Switch

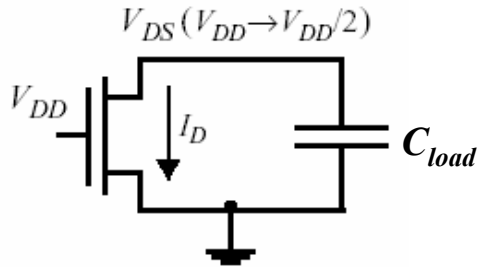
- For digital circuit applications, the MOSFET is either OFF ($V_{GS} < V_T$) or ON ($V_{GS} = V_{DD}$). Thus, we only need to consider two I_D vs. V_{DS} curves:

1. the curve for $V_{GS} < V_T$
2. the curve for $V_{GS} = V_{DD}$



Equivalent Resistance R_{eq}

- In a digital circuit, an n-channel MOSFET in the ON state is typically used to discharge a capacitor connected to its drain terminal:
 - gate voltage $V_G = V_{DD}$
 - source voltage $V_S = 0$ V
 - drain voltage V_D initially at V_{DD} , discharging toward 0 V



The value of R_{eq} should be set to the value which gives the correct propagation delay (time required for output to fall to $\frac{1}{2}V_{DD}$):

$$I_{DSATn} = \frac{k'_n W}{2L} (V_{DD} - V_{Tn})^2 \longrightarrow R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{I_{DSATn}} \left(1 - \frac{5}{6} \lambda_n V_{DD} \right)$$

Typical MOSFET Parameter Values

- For a given MOSFET fabrication process technology, the following parameters are known:
 - V_T (~ 0.5 V)
 - C_{ox} and k' (< 0.001 A/V²)
 - V_{DSAT} (≤ 1 V)
 - λ (≤ 0.1 V⁻¹)

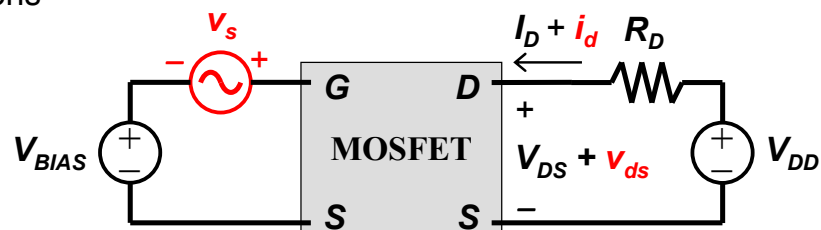
Example R_{eq} values for 0.25 μ m technology ($W = L$):

V_{DD} (V)	1	1.5	2	2.5
NMOS (k Ω)	35	19	15	13
PMOS (k Ω)	115	55	38	31

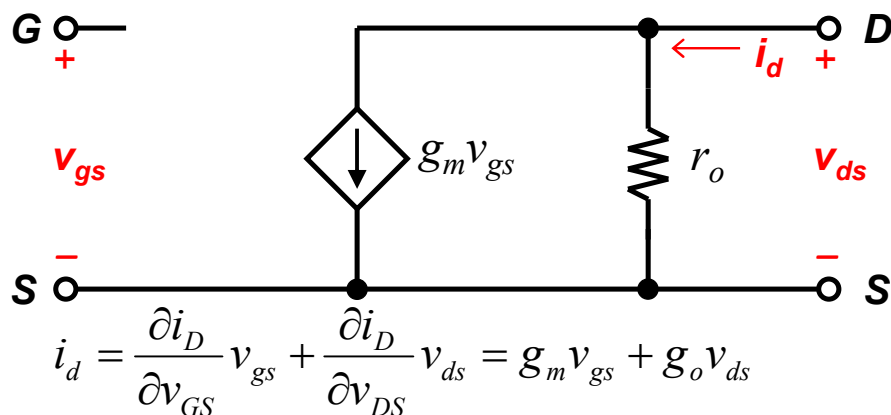
How can R_{eq} be decreased?

MOSFET Model for Analog Circuits

- For analog circuit applications, the MOSFET is biased in the saturation region, and the circuit is designed to process incremental signals.
 - A **DC operating point** is established by the **bias voltages** V_{BIAS} and V_{DD} , such that $V_{DS} > V_{GS} - V_T$
 - Incremental voltages v_s and v_{ds} that are much smaller in magnitude perturb the operating point
 - The MOSFET **small-signal model** is a circuit which models the change in the drain current (i_d) in response to these perturbations



NMOSFET Small-Signal Model



$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \cong \frac{W}{L} k' (V_{GS} - V_T) \quad \text{transconductance}$$

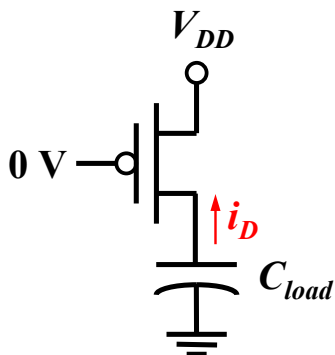
$$g_o \equiv \frac{\partial i_D}{\partial v_{DS}} \cong \lambda I_D \quad \text{output conductance}$$

Notation

- Subscript convention (Lecture 2, Slide 11):
 - $V_{DS} \equiv V_D - V_S$, $V_{GS} \equiv V_G - V_S$, *etc.*
- Double-subscripts denote DC sources (Lecture 23, Slide 7):
 - V_{DD} , V_{CC} , I_{SS} , *etc.*
- To distinguish between DC and AC components of an electrical quantity, the following convention is used:
 - DC quantity: upper-case letter with upper-case subscript
 - I_D , V_{DS} , *etc.*
 - AC quantity: lower-case letter with lower-case subscript
 - i_d , v_{ds} , *etc.*
 - Total (DC + AC) quantity:
 - lower-case letter with upper-case subscript
 - i_D , v_{DS} , *etc.*

P-Channel MOSFET Example

- In a digital circuit, a p-channel MOSFET in the ON state is typically used to charge a capacitor connected to its drain terminal:
 - gate voltage $V_G = 0 \text{ V}$
 - source voltage $V_S = V_{DD}$ (power-supply voltage)
 - drain voltage V_D initially at 0 V , charging toward V_{DD}

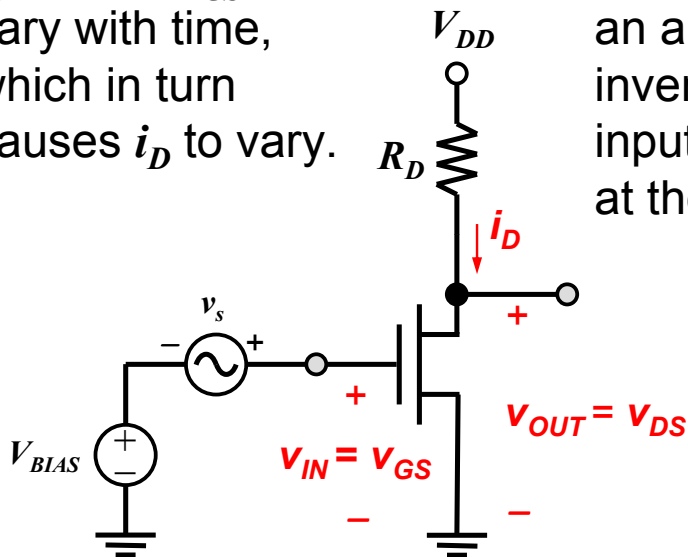


$$R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{|I_{DSATp}|} \left(1 - \frac{5}{6} \lambda_p V_{DD} \right)$$

$$I_{DSAT} = -\frac{k'_p}{2} \frac{W}{L} (V_{DD} - |V_{Tp}|)^2$$

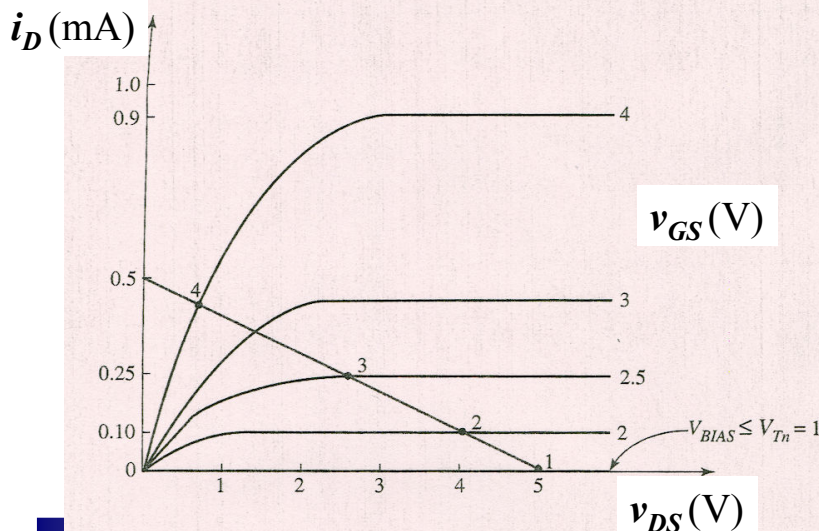
Common-Source (CS) Amplifier

- The input voltage v_s causes v_{GS} to vary with time, which in turn causes i_D to vary.
- The changing voltage drop across R_D causes an amplified (and inverted) version of the input signal to appear at the drain terminal.



Load-Line Analysis of CS Amplifier

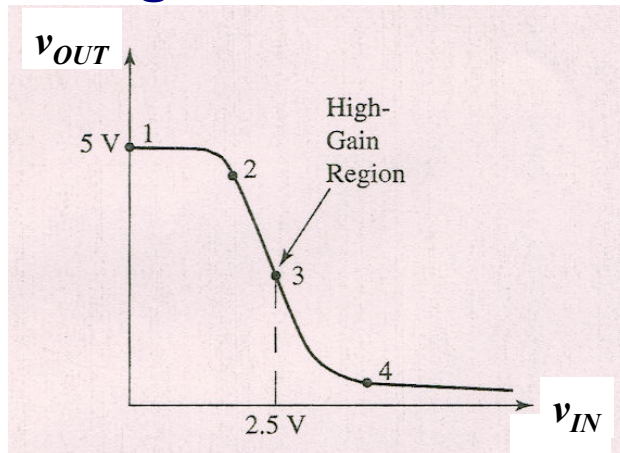
- The operating point of the circuit can be determined by finding the intersection of the appropriate MOSFET i_D vs. v_{DS} characteristic and the load line:



load-line equation:

$$V_{DD} = R_D i_D + v_{DS}$$

Voltage Transfer Function



Goal:

Operate the amplifier in the high-gain region, so that small changes in v_{IN} result in large changes in v_{OUT}

- (1): transistor biased in cutoff region
- (2): $v_{IN} > V_T$; transistor biased in saturation region
- (3): transistor biased in saturation region
- (4): transistor biased in “resistive” or “triode” region

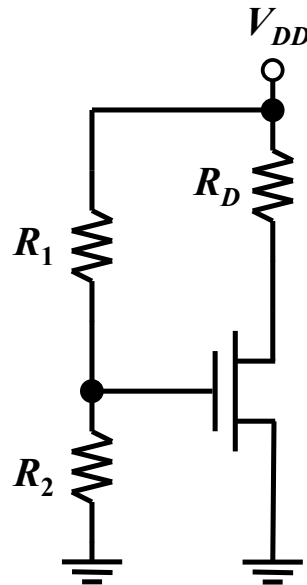
Quiescent Operating Point

- The operating point of the amplifier for zero input signal ($v_s = 0$) is often referred to as the **quiescent operating point** or **Q point**.
 - The Q point should be chosen so that the output voltage is approximately centered between V_{DD} and 0 V.
 - v_s varies the input voltage around the Q point.

Note: The relationship between v_{OUT} and v_{IN} is not linear; this results in a distorted output voltage signal. If the input signal amplitude is very small, however, we can have amplification with negligible distortion.



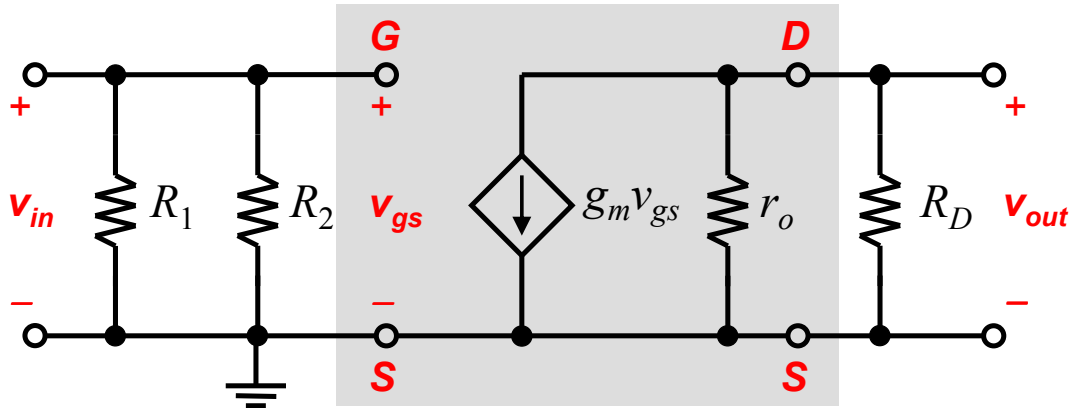
Bias Circuit Example



Rules for Small-Signal Analysis

- A DC supply voltage source acts as a short circuit
 - Even if AC current flows through the DC voltage source, the AC voltage across it is zero.
- A DC supply current source acts as an open circuit
 - Even if AC voltage is applied across the current source, the AC current through it is zero.

Small-Signal Equivalent Circuit



$$v_{out} = -g_m v_{gs} (r_o \parallel R_D)$$

voltage gain $A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \parallel R_D)$

Amplifier Types

1. Voltage amplifier

input & output signals are voltages



2. Current amplifier

input and output signals are currents



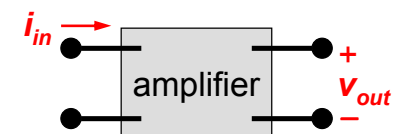
3. Transconductance amplifier

input signal is voltage;
output signal is current

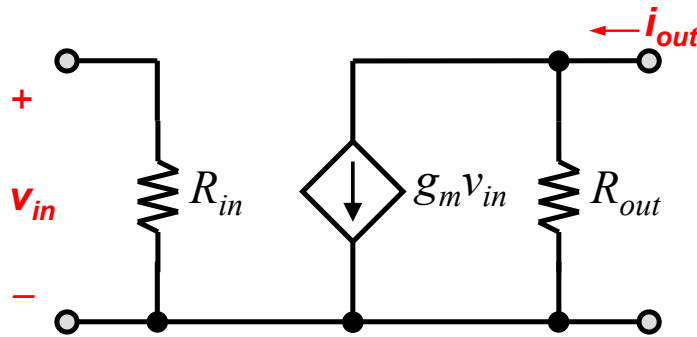


4. Transresistance amplifier

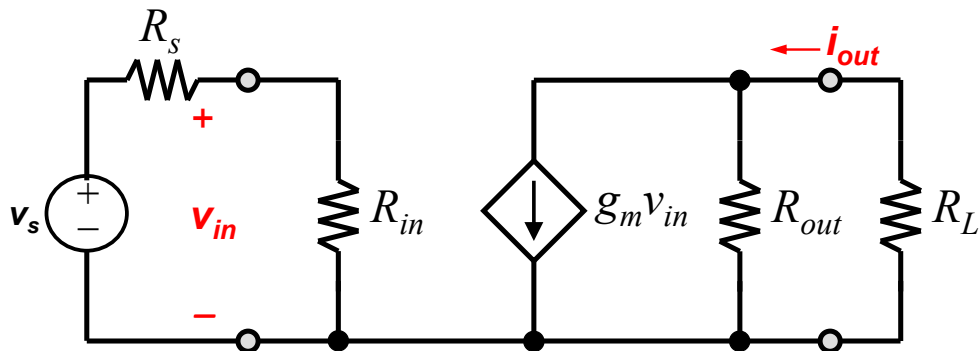
input signal is current;
output signal is voltage



Two-Port Amplifier Model for a transconductance amplifier



Effect of Source and Load Resistances

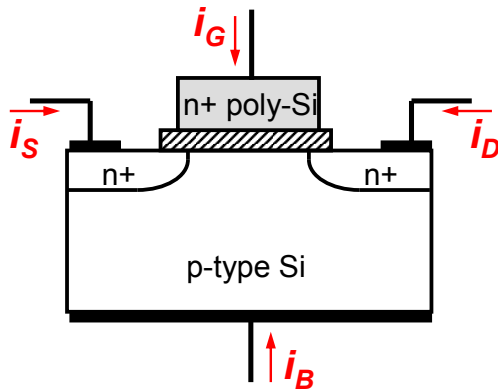


- Overall transconductance is degraded by the source resistance R_s and load resistance R_L

$$\frac{i_{out}}{v_s} = \left(\frac{R_{in}}{R_{in} + R_s} \right) g_m \left(\frac{R_{out}}{R_L + R_{out}} \right)$$

NMOSFET Summary: Current Flow

NMOSFET Structure

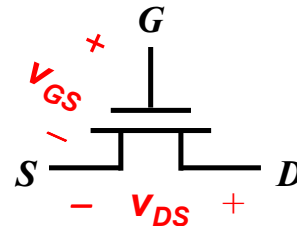


Gate current $i_G = 0$

Body current $i_B = 0$

$$\rightarrow i_S = -i_D$$

NMOSFET Circuit Symbol



If $v_{GS} \leq V_T$, $i_D = 0$

If $v_{GS} > V_T$, $i_D > 0$

Current is limited by either

- the resistance of the inversion-charge layer, or
- velocity saturation

NMOSFET Summary: Modes of Operation

- When $v_{GS} \leq V_T$, an n-type channel is not formed.

\rightarrow No electrons flow from SOURCE to DRAIN

“CUTOFF mode”

- When $v_{GS} > V_T$, an n-type channel (“inversion” layer of electrons at the surface of the semiconductor) is formed.

\rightarrow Electrons may flow from SOURCE to DRAIN ($i_D > 0$)

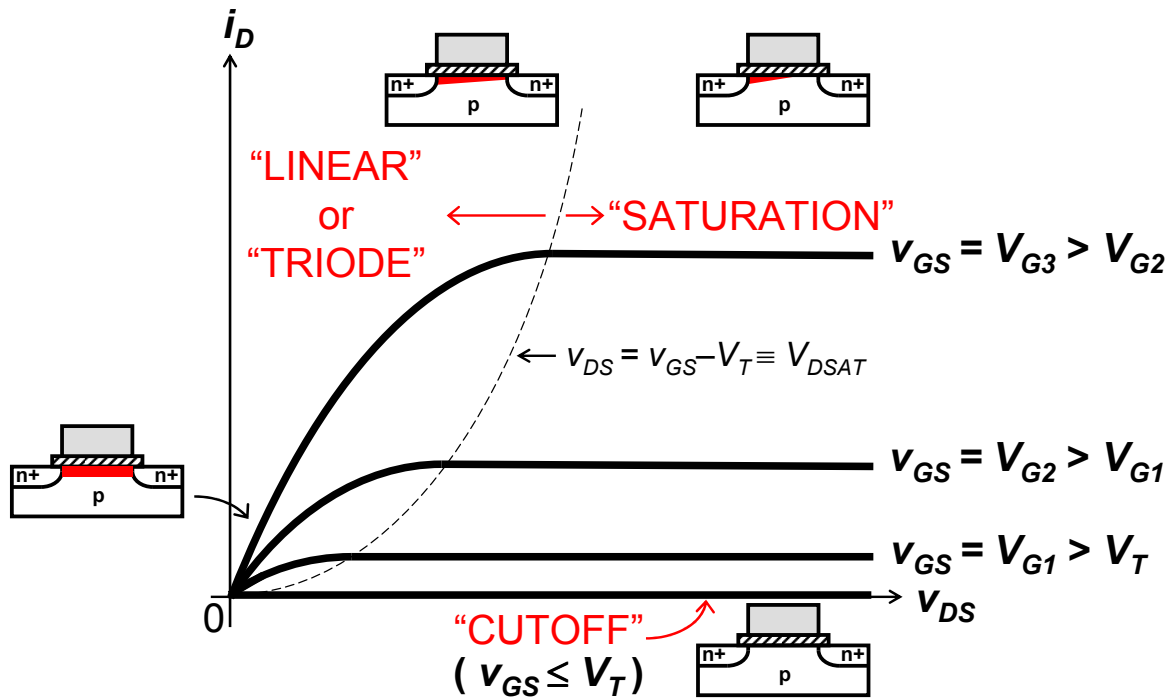
If $v_{DS} < v_{GS} - V_T$, the inversion layer exists across the entire channel length, and current i_D increases with v_{DS}

“LINEAR mode” or “TRIODE mode”

If $v_{DS} \geq v_{GS} - V_T$, the inversion layer is pinched off at the drain end, and current i_D does not increase with v_{DS}

“SATURATION mode”

NMOSFET Summary: I - V Characteristics



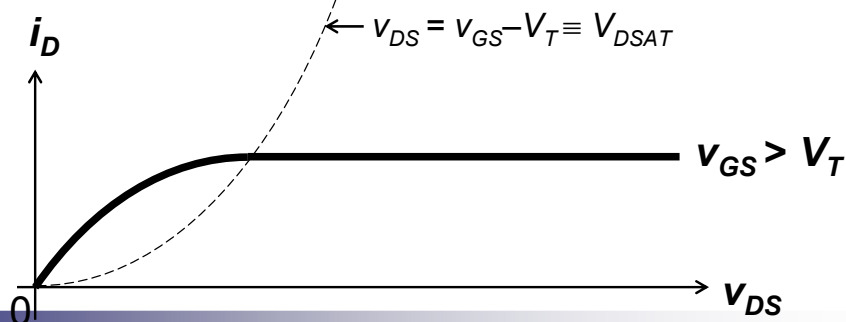
NMOSFET Summary: I - V Equations

"LINEAR" or "TRIODE"

"SATURATION"

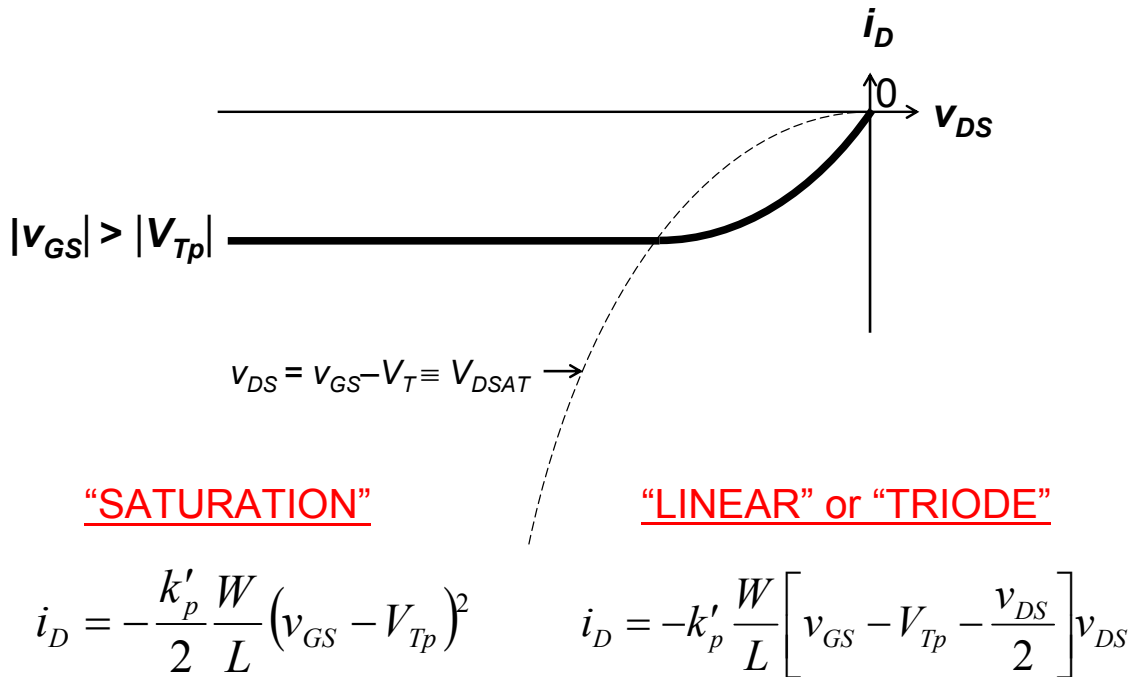
$$i_D = k'_n \frac{W}{L} \left[v_{GS} - V_T - \frac{v_{DS}}{2} \right] v_{DS}$$

$$i_D = \frac{k'_n}{2} \frac{W}{L} (v_{GS} - V_T)^2$$





PMOSFET I - V Equations

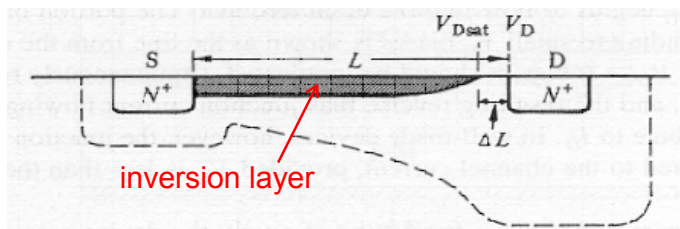


NMOSFET Summary: Non-Ideal Behavior

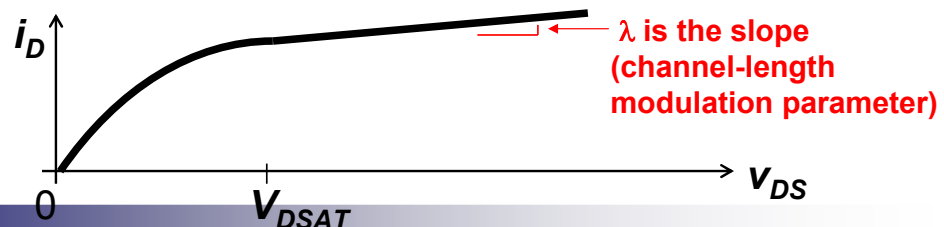
Channel-length modulation:

- The length of the pinch-off region, ΔL , increases with increasing v_{DS} above $v_{GS} - V_T$. It reduces the length of the inversion layer and hence the resistance of this layer.

cross-sectional
view of channel:



→ i_D increases noticeably with v_{DS} , if L is small

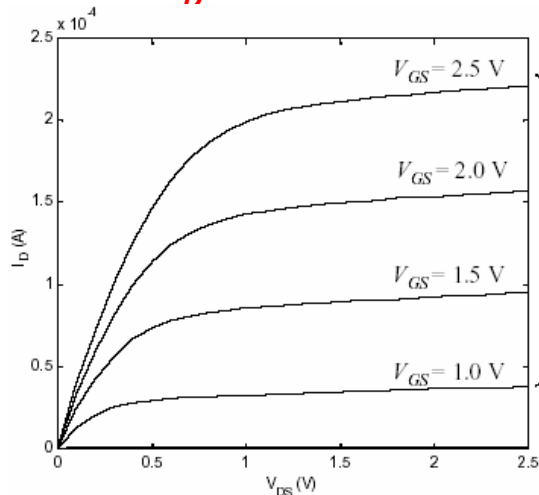


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Velocity Saturation:

- In a very-short-channel MOSFET, i_D saturates because the carrier velocity is limited to $\sim 10^7$ cm/sec

→ i_n reaches a limit before pinch-off occurs



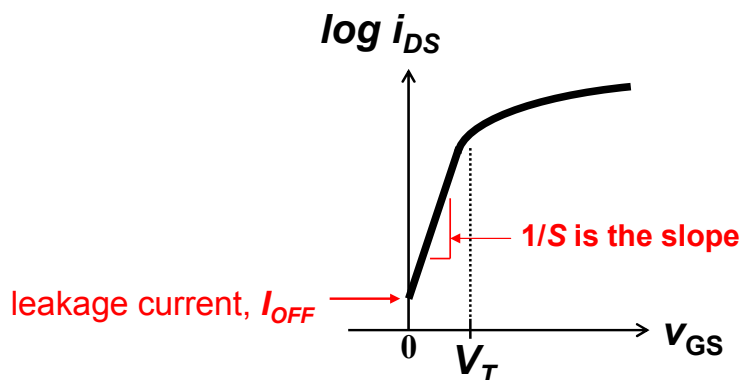
$$i_{DSAT} = WC_{ox} \left[v_{GS} - V_T - \frac{V_{DSAT}}{2} \right] v_{sat}$$

$$\text{where } V_{DSAT} = \frac{L}{\mu_n} v_{sat} < v_{GS} - V_T$$

(continued)

Subthreshold Leakage:

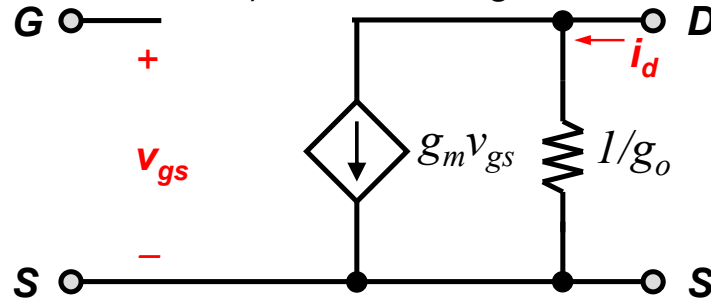
- For $v_{GS} \leq V_T$, i_D is exponentially dependent on v_{GS} :



- The leakage current specification sets the lower limit for the threshold voltage V_T

NMOSFET Summary: Circuit Models

- For analog circuit applications (where we are concerned only with *changes* in current and voltage signals, rather than their total values), the small-signal model is used:

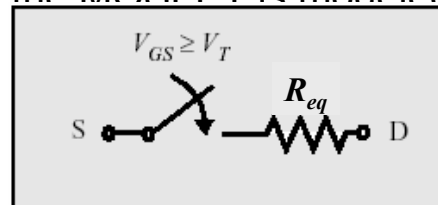
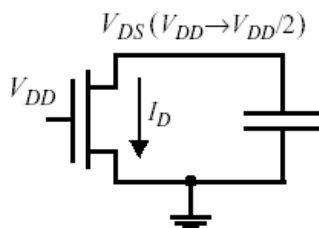


transconductance $g_m \cong \frac{W}{L} k'_n (V_{GS} - V_T)$

output conductance $g_o \cong \lambda I_D$ where V_{GS} & I_D are the DC bias (Q point) values

NMOSFET Summary: Circuit Models

- For digital circuit applications, the MOSFET is modeled as a resistive switch:



$$R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{I_{DSATn}} \left(1 - \frac{5}{6} \lambda_n V_{DD} \right)$$

$$I_{DSATn} = \frac{k'_n}{2} \frac{W}{L} (V_{DD} - V_{Tn})^2$$

