UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EECS 141: Digital Integrated Circuits - Spring 2006

Report Cover Sheet

TERM PROJECT: SRAM Design Cover Sheet

Report 2 – Minimizing Decoder Delay
Due Monday, April 3, 2006 by 10am in drop box.

Names
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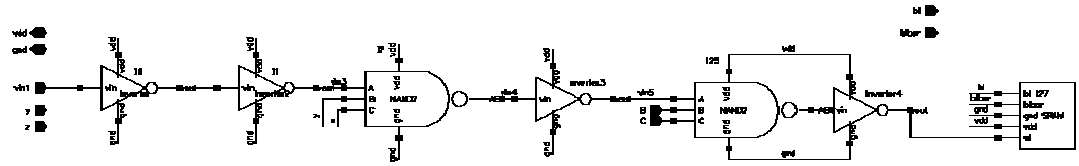
Parameter	Value	Units
Decoder delay (estimate)	670.10	ps
Decoder delay (extracted)	664.45	ps
Wordline capacitance	12.60438	fF

	GRADE
Approach, result and correctness (60%)	
Report (40%)	
TOTAL	

Table of Content

Decoder Design

(annotated schematic and layout of the 6-to-64 decoder, simulated delay waveforms – show delays of each gate in one row explain any differences from the hand design)



Simulation

The worst case delay is 670.1ps.

tplhtot	tphltot	tptot	tplh1
5.604e-10	7.797e-10	6.701e-10	8.331e-11
tphl1	tp1	tplh2	tphl2
6.231e-11	7.281e-11	9.636e-11	9.553e-11
tp2	tplh3	tphl3	tp3
9.594e-11	1.795e-10	8.640e-11	1.330e-10
tplh4	tphl4	tp4	tplh5
1.191e-10	1.203e-10	1.197e-10	1.905e-10
tphl5	tp5	tplh6	tphl6
9.032e-11	1.404e-10	1.059e-10	1.107e-10
tp6	trise	tfall	
1.083e-10	1.888e-10	1.726e-10	

Expected Calculation

tphl = 19.77ps and tplh = 21.80ps, so tp = 20.79ps. According to the delay equation [Rabaey, 255]

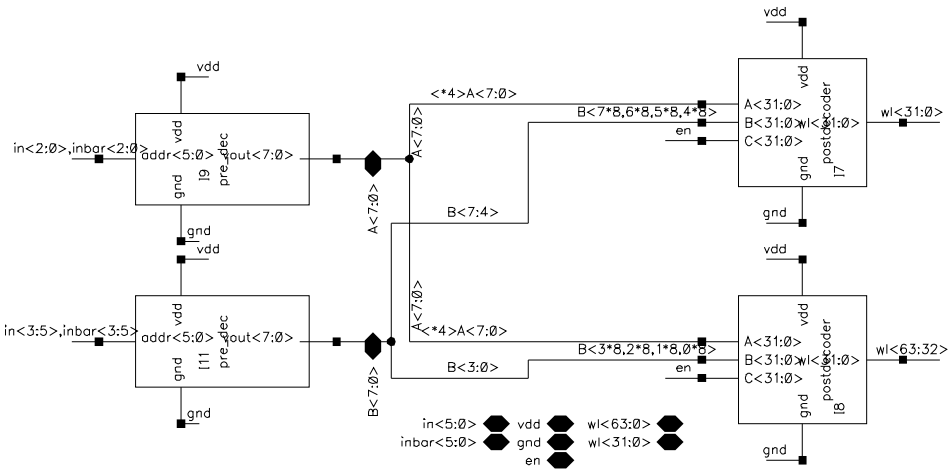
$$D = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right) \text{ where } \gamma = 1$$

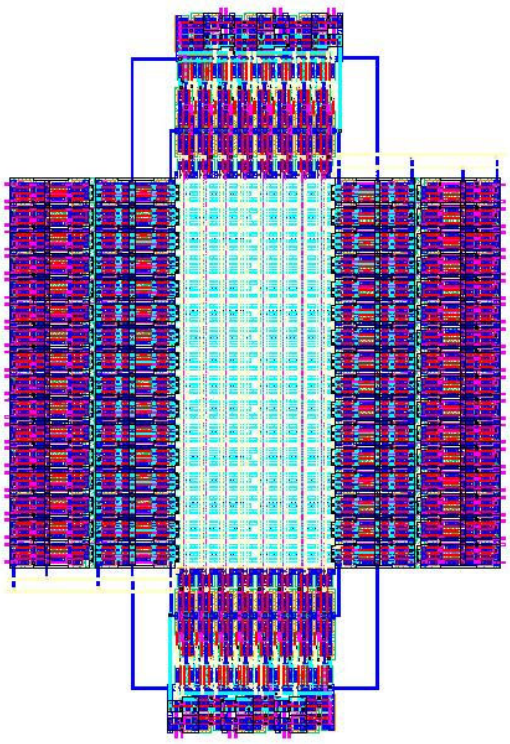
$D = t_{p0}(1+1+3+1+3+1+ 6 * 3.66) = 664.45ps$

Note that the simulated delay is longer than the hand calculation because in the actual layout, the wiring capacitance is everywhere but in the hand calculation, we only considered the one from word line, but we ignore the one after predecoder (NOT-NOT-NAND-NOT). As a result, each gate has larger load to drive, so the simulated delay is longer

(annotated schematic and layout of the 6-to-64 decoder,
simulated delay waweforms – show delays of each gate in one row

explain any differences from the hand design



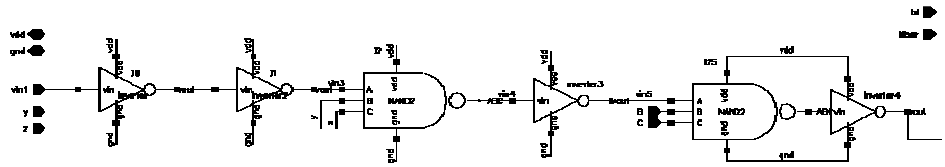


Hand Design of the Decoder

(Wordline capacitance estimation, logic diagram, sizing approach, annotated sizing)

Wordline capcitance

Cw = 12.60438 fF
Cw1 = 1.8641f



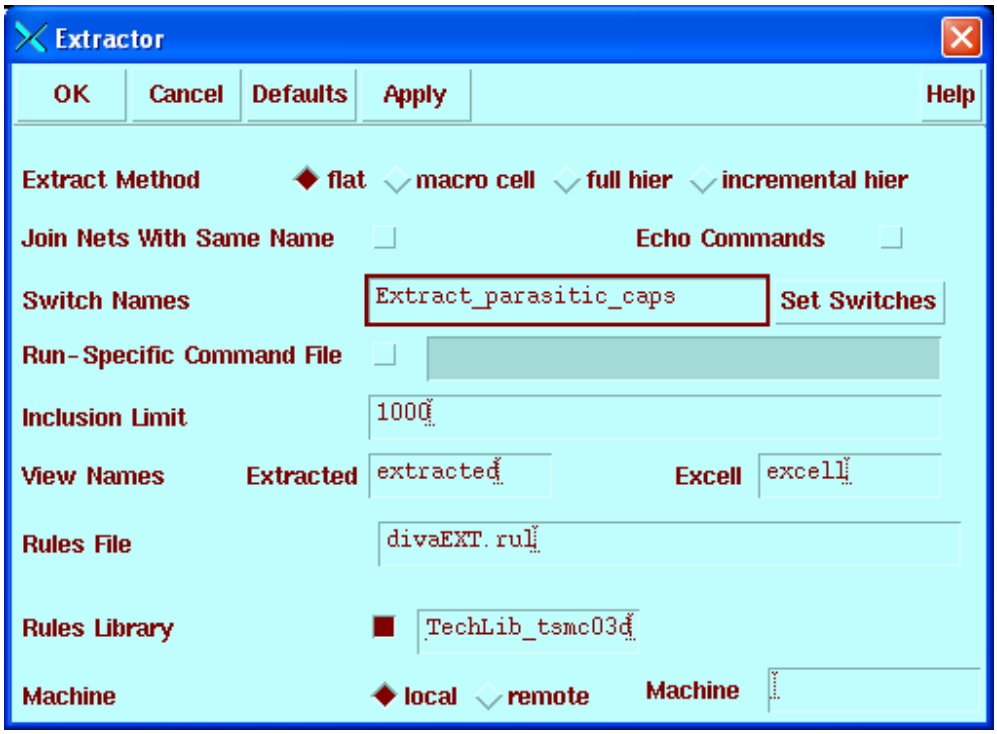
In the prelab, we calculated the path effort, and we found that the optimal stages is 6 with the schematic and sizes above. In the layout we need to make the width and length to the closest multiple of lambdas. Therefore, the widths of pmos and nmos become
The widths for PMOS and NMOS are listed below.
pwidth = 0.7200 2.64 1.5 5.4 1.44 5.34
nwidth = 0.3600 1.32 2.22 2.7 2.16 2.64

Finding Cw

The Load Capacitance depends on the wire capacitance and the gate capacitances of the access transistors. The wire capacitance is extracted from HSPICE. The wire capacitance is 12.60438 fF in this case.

How to extract parasitic capacitance?

Please refer to lab3 tutorial extraction section.
To extract the parasitic capacitance, click on the "Set Switches" and select Extract_parasitic_caps as shown below. That is the only difference from the tutorial in lab 3.



Then just follow the lab 3 tutorial on how to get the netlist.

Cadence to HSPICE Parasitic Extraction for Cw

```
* # FILE NAME: /HOME/AA/UGRAD/BILLHUNG/CADENCE/SIMULATION/TEST/HSPICES/
* EXTRACTED2/NETLIST/TEST.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON MAR 23 20:42:02 2006

C0 75 122 2.01697919999999E-15 M=1.0
C1 75 122 2.0244E-15 M=1.0
C2 75 122 8.56298160000003E-15 M=1.0
M3 145 158 86 145 TSMC25DP L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M4 158 86 145 145 TSMC25DP L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M5 56 60 95 95 TSMC25DP L=240E-9 W=360E-9 AD=273.599990319867E-15
```



```
… (truncated)
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6 M=1
M204 164 122 74 75 TSMC25DN L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9 M=1
M205 68 122 101 75 TSMC25DN L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9 M=1
M206 62 122 5 75 TSMC25DN L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6 M=1

* INCLUDE FILES

* END OF NETLIST
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
.END
```

Gate Capacitance using HSPICE simulation

```
*** input cap
.lib '/home/ff/ee141/MODELS/g25.mod' TT

****************************************
* Parameter
****************************************
.param vddp=2.5
.param vwl=2.5
.param vbl=0
.param vblbar=0
.param cright=.5pF
.param cleft=.5pF

VDD 1 0 'vddp'
M0 2 5 1 1 pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M1 1 2 5 1 pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M2 2 5 0 0 nmos L=240E-9 W=480E-9 AD=165.599996280845E-15
+AS=288.000011209114E-15 PD=779.999993483216E-9 PS=1.67999996847357E-6 M=1
M3 0 2 5 0 nmos L=240E-9 W=480E-9 AD=288.000011209114E-15
+AS=165.599996280845E-15 PD=1.67999996847357E-6 PS=779.999993483216E-9 M=1
M4 4 3 2 0 nmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9 M=1
M5 5 3 6 0 nmos L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6 M=1
Iin 0 3 1u
.ic v(3)=0 v(2)=0
VBLBAR 6 0 0 * first initial condition: both BL and BLBAR are low (but never happen)
VBL 4 0 0
Cblbar 6 0 'cleft'
Cbl 4 0 'cright'

****************************************
* Analysis
****************************************
.options post=2 nomod
.op

.tran 0.01ns 5ns *sweep w 1.08 1.8 .06
.meas t1 trig v(3) val=0.0001 cross=1 targ v(3) val='vddp/2' cross=1
.meas t2 trig v(3) val='vddp/2' cross=1 targ v(3) val='vddp' cross=1

.alter * second initial condition: a read operation, BL and BLBAR are high
VBLBAR 6 0 'vddp'
VBL 4 0 vddp

.alter * third initial condition: a write operation, BL is low and BLBAR is high
VBLBAR 6 0 'vddp'
VBL 4 0 0
.END
```


Finding Effective Fanout h

Finding the effective fanout h of the decoder. The ideal h should be close to four, which should give the optimal delay. Circuit 2 is used in this case, and h is calculated as 3.9175.

Matlab Code Circuit 1 for h

```
%Circuit 1
% 3fF-NOT-NOR-NAND-NOT-Cload
%Parameters
g1=1; g2=7/3; g3=5/3; g4=1;
b1=4; b2=1; b3=8; b4=1;
nstage=6;
%find cload
cw=13.11577; %from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32;
%Find h
G=g1*g2*g3*g4; B=b1*b2*b3*b4; F=(cload)/(3*cg);
H=G*B*F
h=H^(1/nstage)
%Find f
f(1)=h/g1;  f(2)=h/g2;
f(3)=h/g3;  f(4)=h/g4;
%Fing s
s(4)=(cload)/f(4);
s(3)=s(4)/f(3);
s(2)=s(3)/f(2);
s(1)=s(2)*f(1);
```

Output

```
H =  3.3884e+003
h =    3.8756
```

Matlab Code Circuit 2 for h

```
%Circuit 2
% 3fF-NOT-NOT-NAND-NOT-NAND-NOT-Cload
%Parameters
g1=1; g2=7/3; g3=4/3; g4=1; g5=4/3; g6=1;
b1=4; b2=1; b3=8; b4=1; b5=1; b6=1;
nstage=6;
%find cload
cw=13.11577; %from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32;s
%Find h
G=g1*g2*g3*g4*g5*g6; B=b1*b2*b3*b4*b5*b6; F=(cload)/(3*cg);
H=G*B*F
h=H^(1/nstage)
%Find f
f(1)=h/g1; f(2)=h/g2; f(3)=h/g3;
f(4)=h/g4; f(5)=h/g5; f(6)=h/g6;
%Fing s
s(6)=(cload)/f(6);
s(5)=s(6)/f(5); s(4)=s(5)/f(4);
s(3)=s(4)/f(3); s(2)=s(3)/f(2);
s(1)=s(2)*f(1);
```

Output

```
H =  3.6143e+003
h =    3.9175
```


Sizing with cw1 and cload using Matlab (6 stages)

```
%final circuit
%not-not-nand-not-nand-not
% 3fF-NOT-NOT-NAND-NOT-NAND-NOT-Cload
%Parameters
g1=1; g2=1; g3=5/3; g4=1; g5=5/3; g6=1;
b1=1; b2=4; b3=1; b4=8; b5=1; b6=1;
nstage=6;
%find cload
cw=13.11577;
%from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32
%Find h
G=g1*g2*g3*g4*g5*g6; B=b1*b2*b3*b4*b5*b6; F=(cload)/(3*cg);
H=G*B*F
h=H^(1/nstage)
%Find f
f(1)=h/(g1);
f(2)=h/(4*g2);
f(3)=h/g3;
f(4)=h/(8*g4);
f(5)=h/g5;
f(6)=h/g6;
s(6)=(cload)/f(6);
s(5)=s(6)/f(5);  s(4)=s(5)/f(4);
s(3)=s(4)/f(3);  s(2)=s(3)/f(2);
s(1)=s(2)/f(1)



% add cw1
g1=1; g2=1; g3=5/3; g4=1;
b1=1; b2=4; b3=1; b4=1;
nstage2=4;
cw1=1.8641;
cload = s(5)*8+cw1;
F2 = (cload)/(3*cg);
    %cw1 is M4 of the predecoder = 1.8641
B2= b1*b2*b3*b4;
G2 = g1*g2*g3*g4;
H2 = F2* G2* B2
h2 = H2^(1/nstage2)
f1(1)=h2/(b1*g1);
f1(2)=h2/(b2*g2);
f1(3)=h2/(b3*g3);
f1(4)=h2/(b4*g4);
s1(4)=(cload)/f1(4);
s1(3)=s1(4)/f1(3);
s1(2)=s1(3)/f1(2);
s1(1)=s1(2)/f1(1);
%get w
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
inv_min = 3*cg;
nand3_min = 5*cg;
w(6)=s(6)/inv_min;  %did not change
```



```
w(5)=s(5)/nand3_min; %did not change
w(4)=s1(4)/inv_min;
w(3)=s1(3)/nand3_min;
w(2)=s1(2)/inv_min;
w(1)=s1(1)/inv_min

wpmin = 0.72; wnmin = 0.36
pwidth(1) = w(1)*wpmin;
pwidth(2) = w(2)*wpmin;
pwidth(3) = w(3)*wpmin;
pwidth(4) = w(4)*wpmin;
pwidth(5) = w(5)*wpmin;
pwidth(6) = w(6)*wpmin

nwidth(1) = w(1)*wnmin;
nwidth(2) = w(2)*wnmin;
nwidth(3) = 3*w(3)*wnmin;
nwidth(4) = w(4)*wnmin;
nwidth(5) = 3*w(5)*wnmin;
nwidth(6) = w(6)*wnmin
```

Matlab Result

H2 = 185.8524
h2 = 3.6923
w = 1.0000 3.6923 2.0449 7.5504 2.0280 7.4310
pwidth = 0.7200 2.6584 1.4723 5.4363 1.4602 5.3503
nwidth = 0.3600 1.3292 2.2085 2.7181 2.1902 2.6752

Static CMOS Logic HSPICE

HSPICE netlist for the static CMOS decoder design.

test.sp

```
*** phase ii
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'logic.sp'

****************************************
* Parameter
****************************************


Vdd vdd 0 2.5

xinv1 vin1 vin2 vdd 0 INV
xinv2 vin2 vin3 vdd 0 INV M=3.6923

xnand1_b1 vdd 0 vdd vdd vin3 vin4 NAND3 M=2.0449
xnand1_b2 vdd 0 0 0 vin3 x NAND3 M=2.0449
xnand1_b3 vdd 0 0 0 vin3 y NAND3 M=2.0449
xnand1_b4 vdd 0 0 0 vin3 z NAND3 M=2.0449

xinv3 vin4 vin5 vdd 0 INV M=7.5504

xnand2_b1 vdd 0 vdd vdd vin5 vin6 NAND3 M=2.028
xnand2_b2 vdd 0 0 0 vin5 a NAND3 M=2.028
xnand2_b3 vdd 0 0 0 vin5 b NAND3 M=2.028
xnand2_b4 vdd 0 0 0 vin5 c NAND3 M=2.028
xnand2_b5 vdd 0 0 0 vin5 d NAND3 M=2.028
xnand2_b6 vdd 0 0 0 vin5 e NAND3 M=2.028
xnand2_b7 vdd 0 0 0 vin5 f NAND3 M=2.028
xnand2_b8 vdd 0 0 0 vin5 g NAND3 M=2.028
cwire vin5 0 1.8641f

xinv4 vin6 vout vdd 0 INV M=7.431

xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
```

```
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
*cout vout 0 13f
**// analysis
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 10ns 20ns)
.tran 0.1ns 21ns
.options post=2 nomod
.op
.meas tran tplh trig V(vin1) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1

.end
```

logic.sp

```
***
.param wnmin='0.36u'
.param wpmin='2*wnmin'
.subckt INV vin vout vdd vss
M1 vout vin vss vss  nmos l=0.24u w='wnmin'
M2 vout vin vdd vdd  pmos l=0.24u w='wpmin'
.ends

.subckt NAND3 Vdd Gnd VinA VinB VinC Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w='wpmin'
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w='wpmin'
Mp3 Vout VinC Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vmid1 VinA Gnd Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid2 VinB Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vout VinC Vmid2 Gnd nmos l=0.24u w='wnmin*3'
.ends

.subckt Sram Vdd Gnd vword vbit vbitbar
M0 2 5 Vdd Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M1 Vdd 2 5 Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M2 2 5 0 0 nmos L=240E-9 W=480E-9 AD=165.599996280845E-15
+AS=288.000011209114E-15 PD=779.999993483216E-9 PS=1.67999996847357E-6
M=1
M3 0 2 5 0 nmos L=240E-9 W=480E-9 AD=288.000011209114E-15
+AS=165.599996280845E-15 PD=1.67999996847357E-6 PS=779.999993483216E-9
M=1
M4 vbit vword 2 0 nmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9
M=1
M5 5 vword vbitbar 0 nmos L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6
M=1
.ends


*.subckt NOR Vdd Gnd VinA VinB Vout
```

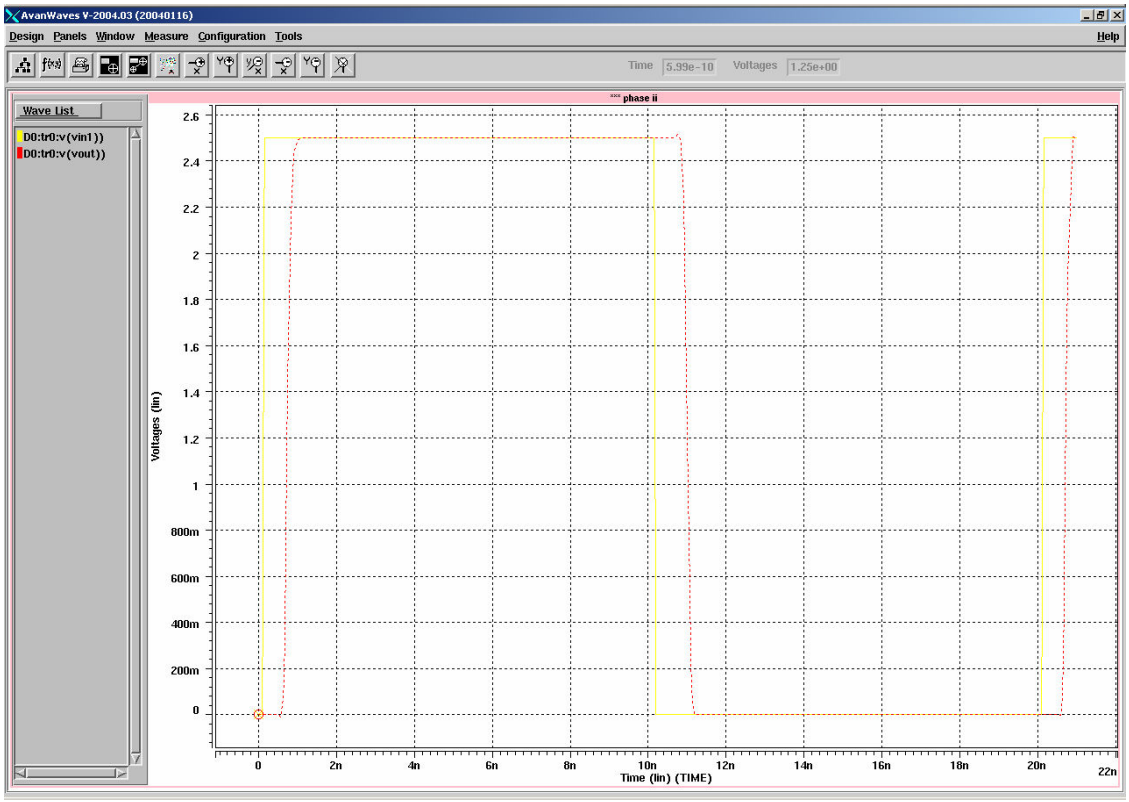
```
*Mp1 Vout VinA Vdd Vdd pmos l=0.24u w=0.6u
*Mp2 Vout VinB Vdd Vdd pmos l=0.24u w=0.6u
*Mn1 Vout VinA vmid Gnd nmos l=0.24u w=0.72u
*Mn2 vmid VinB Gnd Gnd nmos l=0.24u w=0.72u
*.ends
```

Worst scenario

Coming signal arrives at the input gate that is fartherest from the output, which worsen the propagation delay.

```
*** phase ii
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'logic.sp'

****************************************
* Parameter
****************************************
Vdd vdd 0 2.5

xinv1 vin1 vin2 vdd 0 INV
xinv2 vin2 vin3 vdd 0 INV M=3.6923

xnand1_b1 vdd 0 vin3 vdd vdd vin4 NAND3 M=2.0449
xnand1_b2 vdd 0 vin3 vdd vdd x NAND3 M=2.0449
xnand1_b3 vdd 0 vin3 vdd vdd y NAND3 M=2.0449
xnand1_b4 vdd 0 vin3 vdd vdd z NAND3 M=2.0449

xinv3 vin4 vin5 vdd 0 INV M=7.5504

xnand2_b1 vdd 0 vin5 vdd vdd vin6 NAND3 M=2.028
xnand2_b2 vdd 0 vin5 vdd vdd  a NAND3 M=2.028
xnand2_b3 vdd 0 vin5 vdd vdd b NAND3 M=2.028
xnand2_b4 vdd 0 vin5 vdd vdd c NAND3 M=2.028
xnand2_b5 vdd 0 vin5 vdd vdd d NAND3 M= 2.028
xnand2_b6 vdd 0 vin5 vdd vdd e NAND3 M=2.028
xnand2_b7 vdd 0 vin5 vdd vdd f NAND3 M=2.028
xnand2_b8 vdd 0 vin5 vdd vdd g NAND3 M=2.028
cwire vin5 0 1.8641f

xinv4 vin6 vout vdd 0 INV M=7.431

xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
```

```
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
cout vout 0 13f
**// analysis
Vin vin1 0 pulse(0v 2.5v 0.1n 50ps 50ps 10ns 20ns)
.tran 0.1ns 21ns
.options post=2 nomod
.op
.meas tran tplh trig V(vin1) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1
.meas tran trise trig V(vout) val='.1*2.5' rise=1 targ v(vout)
+ val='.9*2.5' rise=1
.end
```



AvanWaves V-2004.03 (20040116)
Design Panels Window Measure Configuration Tools
Help
Time 5.99e-10 Voltages 1.25e+00
Wave List
D0:tr0:v(vin1))
D0:tr0:v(vout))
*** phase ii
Voltages (lin)
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
2n
4n
6n
8n
10n
12n
14n
16n
18n
20n
22n
Time (lin) (TIME)

Sizing with 1.66

L=0.54 for minimum NMOS will gives a gate capacitance close to 3fF.

Sizing 1.66 ratio not-nand-not-nand-not using Matlab (6 stages)

```
g1=1; g2=1; g3=(3+1/.6)/(1+1/.6); g4=1; g5=(3+1/.6)/(1+1/.6); g6=1;
b1=1; b2=4; b3=1; b4=8; b5=1; b6=1;
nstage=6;

%find cload

cw=12.60438;

%from HSPICE extraction
cox=6; co=0.31; w1=0.36; l=0.24;

cga = (cox*l + 2*co)
%gate capacitance of the access transistor
cg = cga*w1;
% wmin for nmos = 0.54, wmin for pmos = 0.9
cin = cga*(.54+.9);

cload = cw + 2*cg*32

%Find h

G=g1*g2*g3*g4*g5*g6; B=b1*b2*b3*b4*b5*b6; F=(cload)/cin;

H=G*B*F

h=H^(1/nstage)

%Find f

f(1)=h/(g1);
f(2)=h/(4*g2);
f(3)=h/g3;

f(4)=h/(8*g4);

f(5)=h/g5;

f(6)=h/g6;

s(6)=(cload)/f(6);

s(5)=s(6)/f(5);

s(4)=s(5)/f(4);

s(3)=s(4)/f(3);

s(2)=s(3)/f(2);
```



```
s(1)=s(2)/f(1);

s

% add cw
F2 = (s(5)*8+1.8641)/cin;
B2= b1*b2*b3;
G2 = g1*g2*g3*g4;
H2 = F2* G2* B2
nstage2 = 4;
h2 = H2^(1/nstage2)
f1(1)=h2/(g1);
f1(2)=h2/(4*g2);
f1(3)=h2/g3;

f1(4)=h2/(g4);

s1(4)=(8*s(5)+1.8641)/f1(4);

s1(3)=s1(4)/f1(3);

s1(2)=s1(3)/f1(2);

s1(1)=s1(2)/f1(1)

invmin = (.9+.54)*cga;
nandmin = (.9+3*.54)*cga;
w(1) = s1(1)/invmin;
w(2) = s1(2)/invmin;
w(3) = s1(3)/nandmin;
w(4) = s1(4)/invmin;
w(5) = s(5)/nandmin;
w(6) = s(6)/invmin



%Find Cg with 1.66 ratio
%cox=6; co=0.31; w1=0.54; l=0.24;
%cg1 = cox*w1*l + 2*co*w1;
%cox=6; co=0.31; w2=w1*1.6666; l=0.24;
%cg2 = cox*w2*l + 2*co*w2;
%cg = cg1+ cg2
```

Matlab Results

cga = 2.0600
cload = 60.0668
H = 1.9844e+003
h = 3.5449
s = 2.9664 10.5156 9.3192 18.8776 8.3649 16.9445
H2 = 162.3128
h2 = 3.5693
s1 = 2.9664 10.5881 9.4481 19.2706
w = 1.0000 3.5693 1.8200 6.4963 1.6114 5.7121

Sizing 1.66 ratio not-nand-not-nand-not using Matlab (5 stages)

```
%g1=1;
g2=1; g3=(3+1/.6)/(1+1/.6); g4=1; g5=(3+1/.6)/(1+1/.6); g6=1;

%b1=1;
b2=4; b3=1; b4=8; b5=1; b6=1;

nstage=5;

%find cload

cw=12.60438;

%from HSPICE extraction
cox=6; co=0.31; w1=0.36; l=0.24;

cga = (cox*l + 2*co)
cg = cga*w1;
cin = cga*(.54+.9);

cload = cw + 2*cg*32

%Find h

G=g2*g3*g4*g5*g6; B=b2*b3*b4*b5*b6; F=(cload)/cin;

H=G*B*F

h=H^(1/nstage)

%Find f

%f(1)=h/(g1);
f(2)=h/(4*g2);
f(3)=h/g3;

f(4)=h/(8*g4);

f(5)=h/g5;

f(6)=h/g6;
f
s(6)=(cload)/f(6);

s(5)=s(6)/f(5);

s(4)=s(5)/f(4);

s(3)=s(4)/f(3);

s(2)=s(3)/f(2);
```

```
%s(1)=s(2)/f(1);


b2=1; b3=4; b4=1
F2 = (s(5)*8+1.8641)/cin;
B2= b2*b3*b4;
G2 = g2*g3*g4;
H2 = F2* G2* B2
nstage2 = 3;
h2 = H2^(1/nstage2)
%f1(1)=h2/(g1);
f1(2)=h2/(4*g2);
f1(3)=h2/g3;

f1(4)=h2/(g4);

s1(4)=(8*s(5)+1.8641)/f1(4);

s1(3)=s1(4)/f1(3);

s1(2)=s1(3)/f1(2);

%s1(1)=s1(2)/f1(1)

s1

invmin = (.9+.54)*cga;
nandmin = (.9+3*.54)*cga;
%w(1) = s1(1)/invmin;
w(2) = s1(2)/invmin;
w(3) = s1(3)/nandmin;
w(4) = s1(4)/invmin;
w(5) = s(5)/nandmin;
w(6) = s(6)/invmin



%Find Cg with 1.66 ratio
%cox=6; co=0.31; w1=0.54; l=0.24;
%cg1 = cox*w1*l + 2*co*w1;
%cox=6; co=0.31; w2=w1*1.6666; l=0.24;
%cg2 = cox*w2*l + 2*co*w2;
%cg = cg1+ cg2
```

Matlab Results

H2 = 99.5860
h2 = 4.6352
s1 = 0 2.9664 3.4374 9.1047
w = 0 1.0000 0.6622 3.0693 0.9713 4.4348

HSPICE Simulation

Gate.sp

```
*w =    1.0000    3.5693    1.8200    6.4963    1.6114    5.7121
*Lmin= 0.54u

.param wnmin='0.54u'
.param wpmin='1.66*wnmin'

.subckt INV vin vout vdd vss
M1 vout vin vss vss  nmos l=0.24u w='wnmin'
M2 vout vin vdd vdd  pmos l=0.24u w='wpmin'
.ends

.subckt NAND3 Vdd Gnd VinA VinB VinC Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w='wpmin'
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w='wpmin'
Mp3 Vout VinC Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vmid1 VinA Gnd Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid2 VinB Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vout VinC Vmid2 Gnd nmos l=0.24u w='wnmin*3'
.ends

.subckt Sram Vdd Gnd vword vbit vbitbar
   *M<name> <drain> <gate> <source> <bulk> <model> <geometry>
M0 2 5 Vdd Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M1 Vdd 2 5 Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M2 2 5 0 0 nmos L=240E-9 W=480E-9 AD=165.599996280845E-15
+AS=288.000011209114E-15 PD=779.999993483216E-9 PS=1.67999996847357E-6
M=1
M3 0 2 5 0 nmos L=240E-9 W=480E-9 AD=288.000011209114E-15
+AS=165.599996280845E-15 PD=1.67999996847357E-6 PS=779.999993483216E-9
M=1
M4 vbit vword 2 0 nmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9
M=1
M5 5 vword vbitbar 0 nmos L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6
M=1
.ends


.subckt NOR Vdd Gnd VinA VinB Vout
```



```
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w=0.6u
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w=0.6u
Mn1 Vout VinA vmid Gnd nmos l=0.24u w=0.72u
Mn2 vmid VinB Gnd Gnd nmos l=0.24u w=0.72u
.ends

.subckt DNAND3 Vdd Gnd VinA VinB VinC Vout Clk keep
Mclk1 Vout Clk Vdd Vdd pmos l=0.24u w='wpmin'
Mkp Vout keep Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vout VinA Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid1 VinB Vmid2 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vmid2 VinC Vmid3 Gnd nmos l=0.24u w='wnmin*3'
Mclk2 Vmid3 Clk Gnd Gnd nmos  l=0.24u w='wnmin*3'
.ends
```

sixStatic.sp

```
STATIC 6 STAGES

.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'logic.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_inv1 = 3.5693
.param multi_nand1 = 1.820
.param multi_inv2 = 6.4963
.param multi_nand3 = 1.6114
.param multi_inv3 = 5.7121
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin0 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************
xinv0 vin0 vin1 vdd 0 INV
xinv1 vin1 vin2 vdd 0 INV M='multi_inv1'
xnand1_b1 vdd 0 vdd vdd vin2 vin3 NAND3 M='multi_nand1'
xnand1_b2 vdd 0 0 0 vin2 x NAND3 M='multi_nand1'
xnand1_b3 vdd 0 0 0 vin2 y NAND3 M='multi_nand1'
xnand1_b4 vdd 0 0 0 vin2 z NAND3 M='multi_nand1'
```

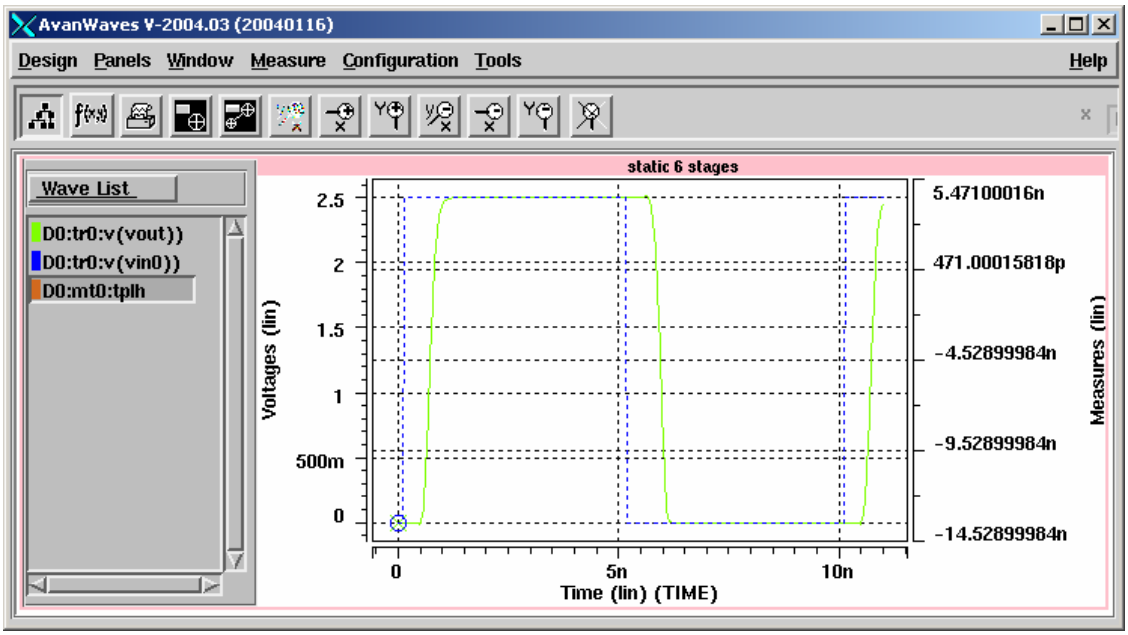


```
xinv2 vin3 vin4 vdd 0 INV M='multi_inv2'
cw1 vin5 0 1.8641f
xnand2_b1 vdd 0 vdd vdd vin4 vin5 NAND3 M='multi_nand3'
xnand2_b2 vdd 0 0 0 vin5 a NAND3 M='multi_nand3'
xnand2_b3 vdd 0 0 0 vin5 b NAND3 M='multi_nand3'
xnand2_b4 vdd 0 0 0 vin5 c NAND3 M='multi_nand3'
xnand2_b5 vdd 0 0 0 vin5 d NAND3 M='multi_nand3'
xnand2_b6 vdd 0 0 0 vin5 e NAND3 M='multi_nand3'
xnand2_b7 vdd 0 0 0 vin5 f NAND3 M='multi_nand3'
xnand2_b8 vdd 0 0 0 vin5 g NAND3 M='multi_nand3'
xinv3 vin5 vout vdd 0 INV M='multi_inv3'
cload vout 0 12.60438fF

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
```



```
xsram31 vdd 0 vout vbit31 vbitbar31 Sram
cout vout 0 13f

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op

.tran 0.01ns 11ns * sweep multi_nand3 9.27 11.27 1
.meas tran tplh trig V(vin0) val='(2.5*.5)' rise=1 targ V(vout)
+ val='(2.5*.5)' rise=1
.end
```

Awaves Result




```
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03       '
.TITLE 'static 6 stages'
 tplh             temper          alter#
  6.061e-10        25.0000          1.0000
```

Static 2-1 Ratio (6 Stages)

HSPICE – sixStatic2.sp

STATIC 6 STAGES 2-1 ratio

```
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'gate2.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_inv0 = 1
.param multi_inv1 = 3.6923
.param multi_nand1 = 2.0449
.param multi_inv2 = 7.5504
.param multi_nand2 = 2.028
.param multi_inv3 = 7.431
.param cw1_value  = 1.8641fF
.param cload_value =12.60438fF
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin0 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************
xinv0 vin0 vin1 vdd 0 INV M='multi_inv0'
xinv1 vin1 vin2 vdd 0 INV M='multi_inv1'
xnand1_b1 vdd 0 vin2 vin2 vin2 vin3 NAND3 M='multi_nand1'
xnand1_b2 vdd 0 vin2 0 0 x NAND3 M='multi_nand1'
xnand1_b3 vdd 0 vin2 0 0 y NAND3 M='multi_nand1'
xnand1_b4 vdd 0 vin2 0 0  z NAND3 M='multi_nand1'
xinv2 vin3 vin4 vdd 0 INV M='multi_inv2'
cw1 vin4 0 'cw1_value'
xnand2_b1 vdd 0 vin4 vin4 vin4 vin5 NAND3 M='multi_nand2'
xnand2_b2 vdd 0 vin4 0 0 a NAND3 M='multi_nand2'
xnand2_b3 vdd 0 vin4 0 0 b NAND3 M='multi_nand2'
xnand2_b4 vdd 0 vin4 0 0 c NAND3 M='multi_nand2'
xnand2_b5 vdd 0 vin4 0 0 d NAND3 M='multi_nand2'
xnand2_b6 vdd 0 vin4 0 0 e NAND3 M='multi_nand2'
xnand2_b7 vdd 0 vin4 0 0 f NAND3 M='multi_nand2'
```

```
xnand2_b8 vdd 0 vin4 0 0 g NAND3 M='multi_nand2'
xinv3 vin5 vout vdd 0 INV M='multi_inv3'
cload vout 0 'cload_value'

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op
```



```
.tran 0.01ns 16ns  sweep multi_nand2 0.028 2.028 0.25
.meas tran tplh trig V(vin0) val='2.5*.5' rise=1 targ V(vout)
+ val='2.5*.5' rise=1
.meas tran tphl trig V(vin0) val='2.5*.5' fall=1 targ V(vout)
+val='2.5*.5' fall=1
.meas tran tp param='(tphl+tplh)/2'
.meas tran rise_time trig V(vout) val='.1*2.5' rise=1 targ v(vout)
+val='.9*2.5' rise=1
.meas tran fall_time trig V(vout) val='.9*2.5' fall=1 targ v(vout)
+val='.1*2.5' fall=1

.end
```

Gate2.sp

```
.param wnmin='0.36u'
.param wpmin='2*wnmin'


.subckt INV vin vout vdd vss
M1 vout vin vss vss  nmos l=0.24u w='wnmin'
M2 vout vin vdd vdd  pmos l=0.24u w='wpmin'
.ends



.subckt Sram Vdd Gnd vword vbit vbitbar
   *M<name> <drain> <gate> <source> <bulk> <model> <geometry>
M0 2 5 Vdd Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M1 Vdd 2 5 Vdd pmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=273.599990319867E-15 PD=1.7999999499807E-6 PS=1.7999999499807E-6 M=1
M2 2 5 0 0 nmos L=240E-9 W=480E-9 AD=165.599996280845E-15
+AS=288.000011209114E-15 PD=779.999993483216E-9 PS=1.67999996847357E-6
M=1
M3 0 2 5 0 nmos L=240E-9 W=480E-9 AD=288.000011209114E-15
+AS=165.599996280845E-15 PD=1.67999996847357E-6 PS=779.999993483216E-9
M=1
M4 vbit vword 2 0 nmos L=240E-9 W=360E-9 AD=273.599990319867E-15
+AS=165.599996280845E-15 PD=1.7999999499807E-6 PS=779.999993483216E-9
M=1
M5 5 vword vbitbar 0 nmos L=240E-9 W=360E-9 AD=165.599996280845E-15
+AS=273.599990319867E-15 PD=779.999993483216E-9 PS=1.7999999499807E-6
M=1
.ends
```

```
.subckt NOR Vdd Gnd VinA VinB Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w=0.6u
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w=0.6u
Mn1 Vout VinA vmid Gnd nmos l=0.24u w=0.72u
Mn2 vmid VinB Gnd Gnd nmos l=0.24u w=0.72u
.ends

.subckt NAND3 Vdd Gnd VinA VinB VinC Vout
Mp1 Vout VinA Vdd Vdd pmos l=0.24u w='wpmin'
Mp2 Vout VinB Vdd Vdd pmos l=0.24u w='wpmin'
Mp3 Vout VinC Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vmid1 VinA Gnd Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid2 VinB Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vout VinC Vmid2 Gnd nmos l=0.24u w='wnmin*3'
.ends

.subckt DNAND3 Vdd Gnd VinA VinB VinC Vout Clk keep
Mclk1 Vout Clk Vdd Vdd pmos l=0.24u w='wpmin'
Mkp Vout keep Vdd Vdd pmos l=0.24u w='wpmin'
Mn1 Vout VinA Vmid1 Gnd nmos l=0.24u w='wnmin*3'
Mn2 Vmid1 VinB Vmid2 Gnd nmos l=0.24u w='wnmin*3'
Mn3 Vmid2 VinC Vmid3 Gnd nmos l=0.24u w='wnmin*3'
Mclk2 Vmid3 Clk Gnd Gnd nmos  l=0.24u w='wnmin*3'
.ends
```

HSPICE Result

```
multi_nand2      tplh           tphl           tp
            rise_time       fall_time       temper
            alter#
 2.0280       7.070e-10       5.233e-10       6.152e-10
             1.839e-10       1.120e-10       25.0000
               1.0000
```

5 Stages? Or 6 Stages?

```
g1=1; g2=1; g3=5/3; g4=1; g5=5/3; g6=1;
b1=1; b2=4; b3=1; b4=8; b5=1; b6=1;
nstage=6;
%find cload
cw=13.11577;
%from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32
%Find h
G=g1*g2*g3*g4*g5*g6; B=b1*b2*b3*b4*b5*b6; F=(cload)/(3*cg);
H=G*B*F
```

```
>> tpo=20; p=9; N=5; H=2420.3; gamma=1;
D = tpo*(p+N*(H^(1/N))/gamma)

D =

  655.0878

>> tpo=20; p=10; N=6; H=2420.3; gamma=1;
D = tpo*(p+N*(H^(1/N))/gamma)

D =

  639.7030
```

6 Stage is better according to the equation on page 255.

Sweeping 8 Nand-Gate Sizes

```
.TITLE 'static 6 stages 2-1 ratio'
 multi_nand2      tplh             tphl             tp
                  rise_time        fall_time        temper
                  alter#
  2.800e-02        3.478e-09        1.401e-09        2.440e-09
                   1.710e-09        9.114e-10         25.0000
                     1.0000
    0.2780         8.870e-10        6.067e-10        7.468e-10
                   2.971e-10        1.827e-10         25.0000
                     1.0000
    0.5280         7.496e-10        5.394e-10        6.445e-10
                   2.346e-10        1.513e-10         25.0000
                     1.0000
    0.7780         7.159e-10        5.198e-10        6.178e-10
                   2.166e-10        1.389e-10         25.0000
                     1.0000
    1.0280         6.988e-10        5.135e-10        6.062e-10
                   2.053e-10        1.276e-10         25.0000
                     1.0000
    1.2780         6.964e-10        5.117e-10        6.040e-10
                   1.927e-10        1.184e-10         25.0000
                     1.0000
    1.5280         6.958e-10        5.167e-10        6.063e-10
                   1.902e-10        1.205e-10         25.0000
                     1.0000
    1.7780         7.008e-10        5.192e-10        6.100e-10
                   1.882e-10        1.177e-10         25.0000
                     1.0000
    2.0280         7.070e-10        5.233e-10        6.152e-10
                   1.839e-10        1.120e-10         25.0000
                     1.0000
```

Final Sizing Test

```
STATIC 6 STAGES 2-1 ratio

.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'gate2.sp'

****************************************
* Parameter
****************************************
.param vddp = 2.5
.param multi_inv0 = 1
.param multi_inv1 = 3.6923
.param multi_nand1 = 2.0449
.param multi_inv2 = 7.5504
.param multi_nand2 = 2.028
.param multi_inv3 = 7.431
.param cw1_value  = 1.8641fF
.param cload_value =12.60438fF
****************************************
* Sources
****************************************
Vdd vdd 0 'vddp'
* params = vlow vhigh delay rise fall pulse_width period
* example VIN IN GND PULSE 0 5 .5n .1n .1n .5n 2n
Vin vin0 0 pulse(0v 2.5v 0.1n 50ps 50ps 5ns 10ns)
****************************************
* Netlist
****************************************
xinv0 vin0 vin1 vdd 0 INV M='multi_inv0'
xinv1 vin1 vin2 vdd 0 INV M='multi_inv1'
xnand1_b1 vdd 0 vin2 vin2 vin2 vin3 NAND3 M='multi_nand1'
xnand1_b2 vdd 0 vin2 0 0 x NAND3 M='multi_nand1'
xnand1_b3 vdd 0 vin2 0 0 y NAND3 M='multi_nand1'
xnand1_b4 vdd 0 vin2 0 0  z NAND3 M='multi_nand1'
xinv2 vin3 vin4 vdd 0 INV M='multi_inv2'
cw1 vin4 0 'cw1_value'
xnand2_b1 vdd 0 vin4 vin4 vin4 vin5 NAND3 M='multi_nand2'
xnand2_b2 vdd 0 vin4 0 0 a NAND3 M='multi_nand2'
xnand2_b3 vdd 0 vin4 0 0 b NAND3 M='multi_nand2'
xnand2_b4 vdd 0 vin4 0 0 c NAND3 M='multi_nand2'
xnand2_b5 vdd 0 vin4 0 0 d NAND3 M='multi_nand2'
xnand2_b6 vdd 0 vin4 0 0 e NAND3 M='multi_nand2'
xnand2_b7 vdd 0 vin4 0 0 f NAND3 M='multi_nand2'
xnand2_b8 vdd 0 vin4 0 0 g NAND3 M='multi_nand2'
xinv3 vin5 vout vdd 0 INV M='multi_inv3'
cload vout 0 'cload_value'

* SRAM Chain
xsram0 vdd 0 vout vbit0 vbitbar0 Sram
xsram1 vdd 0 vout vbit1 vbitbar1 Sram
xsram2 vdd 0 vout vbit2 vbitbar2 Sram
xsram3 vdd 0 vout vbit3 vbitbar3 Sram
xsram4 vdd 0 vout vbit4 vbitbar4 Sram
xsram5 vdd 0 vout vbit5 vbitbar5 Sram
xsram6 vdd 0 vout vbit6 vbitbar6 Sram
xsram7 vdd 0 vout vbit7 vbitbar7 Sram
xsram8 vdd 0 vout vbit8 vbitbar8 Sram
xsram9 vdd 0 vout vbit9 vbitbar9 Sram
xsram10 vdd 0 vout vbit10 vbitbar10 Sram
```



```
xsram11 vdd 0 vout vbit11 vbitbar11 Sram
xsram12 vdd 0 vout vbit12 vbitbar12 Sram
xsram13 vdd 0 vout vbit13 vbitbar13 Sram
xsram14 vdd 0 vout vbit14 vbitbar14 Sram
xsram15 vdd 0 vout vbit15 vbitbar15 Sram
xsram16 vdd 0 vout vbit16 vbitbar16 Sram
xsram17 vdd 0 vout vbit17 vbitbar17 Sram
xsram18 vdd 0 vout vbit18 vbitbar18 Sram
xsram19 vdd 0 vout vbit19 vbitbar19 Sram
xsram20 vdd 0 vout vbit20 vbitbar20 Sram
xsram21 vdd 0 vout vbit21 vbitbar21 Sram
xsram22 vdd 0 vout vbit22 vbitbar22 Sram
xsram23 vdd 0 vout vbit23 vbitbar23 Sram
xsram24 vdd 0 vout vbit24 vbitbar24 Sram
xsram25 vdd 0 vout vbit25 vbitbar25 Sram
xsram26 vdd 0 vout vbit26 vbitbar26 Sram
xsram27 vdd 0 vout vbit27 vbitbar27 Sram
xsram28 vdd 0 vout vbit28 vbitbar28 Sram
xsram29 vdd 0 vout vbit29 vbitbar29 Sram
xsram30 vdd 0 vout vbit30 vbitbar30 Sram
xsram31 vdd 0 vout vbit31 vbitbar31 Sram

****************************************
* Analysis
****************************************
*nomod= no model info from library
.options post=2 nomod
*.op makes hspice determines DC operating point
.op

.tran 0.01ns 16ns
* sweep multi_nand2 0.028 2.028 0.25
.meas tran tplh trig V(vin0) val='2.5*.5' rise=1 targ V(vout)
+ val='2.5*.5' rise=1
.meas tran tphl trig V(vin0) val='2.5*.5' fall=1 targ V(vout)
+val='2.5*.5' fall=1
.meas tran tp param='(tphl+tplh)/2'
.meas tran rise_time trig V(vout) val='.1*2.5' rise=1 targ v(vout)
+val='.9*2.5' rise=1
.meas tran fall_time trig V(vout) val='.9*2.5' fall=1 targ v(vout)
+val='.1*2.5' fall=1


.alter
.param multi_nand2=2.528
.param multi_inv3=7.931
.alter
.param multi_nand2=1.528
.param multi_inv3=7.931
.alter
.param multi_nand2=2.528
.param multi_inv3=6.931
.alter
.param multi_nand2=1.528
.param multi_inv3=6.931


.end
```

HSPICE Result

```
> cat sixStatic2.mt0
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03      '
.TITLE 'static 6 stages 2-1 ratio'
 tplh          tphl          tp            rise_time
 fall_time     temper        alter#
  7.070e-10     5.233e-10     6.152e-10     1.839e-10
  1.120e-10     25.0000       1.0000
> cat sixStatic2.mt1
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03      '
.TITLE 'static 6 stages 2-1 ratio'
 tplh          tphl          tp            rise_time
 fall_time     temper        alter#
  7.218e-10     5.326e-10     6.272e-10     1.864e-10
  1.090e-10     25.0000       2.0000
> cat sixStatic2.mt2
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03      '
.TITLE 'static 6 stages 2-1 ratio'
 tplh          tphl          tp            rise_time
 fall_time     temper        alter#
  6.969e-10     5.167e-10     6.068e-10     1.870e-10
  1.183e-10     25.0000       3.0000
> cat sixStatic2.mt3
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03      '
.TITLE 'static 6 stages 2-1 ratio'
 tplh          tphl          tp            rise_time
 fall_time     temper        alter#
  7.208e-10     5.343e-10     6.276e-10     1.896e-10
  1.160e-10     25.0000       4.0000
> cat sixStatic2.mt4
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03      '
.TITLE 'static 6 stages 2-1 ratio'
 tplh          tphl          tp            rise_time
 fall_time     temper        alter#
  6.951e-10     5.157e-10     6.054e-10     1.941e-10
  1.170e-10     25.0000       5.0000
```

Since the delay only improve by 10ps, we decided to use the sizing we calculated using MatLab.

Final Sizing Width with Matlab

```
%final circuit
%not-not-nand-not-nand-not
% 3fF-NOT-NOT-NAND-NOT-NAND-NOT-Cload
%Parameters
g1=1; g2=1; g3=5/3; g4=1; g5=5/3; g6=1;
b1=1; b2=4; b3=1; b4=8; b5=1; b6=1;
nstage=6;
%find cload
cw=13.11577;
%from HSPICE extraction
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
cload = cw + 2*cg*32
%Find h
G=g1*g2*g3*g4*g5*g6; B=b1*b2*b3*b4*b5*b6; F=(cload)/(3*cg);
H=G*B*F
h=H^(1/nstage)
%Find f
f(1)=h/(g1);
f(2)=h/(4*g2);
f(3)=h/g3;
f(4)=h/(8*g4);
f(5)=h/g5;
f(6)=h/g6;
s(6)=(cload)/f(6);
s(5)=s(6)/f(5);  s(4)=s(5)/f(4);
s(3)=s(4)/f(3);  s(2)=s(3)/f(2);
s(1)=s(2)/f(1)



% add cw1
g1=1; g2=1; g3=5/3; g4=1;
b1=1; b2=4; b3=1; b4=1;
nstage2=4;
cw1=1.8641;
cload = s(5)*8+cw1;
F2 = (cload)/(3*cg);
%cw1 is M4 of the predecoder = 1.8641
B2= b1*b2*b3*b4;
G2 = g1*g2*g3*g4;
H2 = F2* G2* B2
h2 = H2^(1/nstage2)
f1(1)=h2/(b1*g1);
f1(2)=h2/(b2*g2);
f1(3)=h2/(b3*g3);
f1(4)=h2/(b4*g4);
s1(4)=(cload)/f1(4);
s1(3)=s1(4)/f1(3);
s1(2)=s1(3)/f1(2);
s1(1)=s1(2)/f1(1);
%get w
cox=6; co=0.31; w=0.36; l=0.24;
cg = cox*w*l + 2*co*w;
inv_min = 3*cg;
nand3_min = 5*cg;
w(6)=s(6)/inv_min;  %did not change
```



```
w(5)=s(5)/nand3_min; %did not change
w(4)=s1(4)/inv_min;
w(3)=s1(3)/nand3_min;
w(2)=s1(2)/inv_min;
w(1)=s1(1)/inv_min

wpmin = 0.72; wnmin = 0.36
pwidth(1) = w(1)*wpmin;
pwidth(2) = w(2)*wpmin;
pwidth(3) = w(3)*wpmin;
pwidth(4) = w(4)*wpmin;
pwidth(5) = w(5)*wpmin;
pwidth(6) = w(6)*wpmin;

nwidth(1) = w(1)*wnmin;
nwidth(2) = w(2)*wnmin;
nwidth(3) = 3*w(3)*wnmin;
nwidth(4) = w(4)*wnmin;
nwidth(5) = 3*w(5)*wnmin;
nwidth(6) = w(6)*wnmin;
```

Matlab Results

w = 1.0000 3.6923 2.0449 7.5504 2.0280 7.4310
wnmin = 0.3600
>> pwidth
pwidth =
0.7200 2.6584 1.4723 5.4363 1.4602 5.3503
>> nwidth
nwidth = 0.3600 1.3292 2.2085 2.7181 2.1902 2.6752

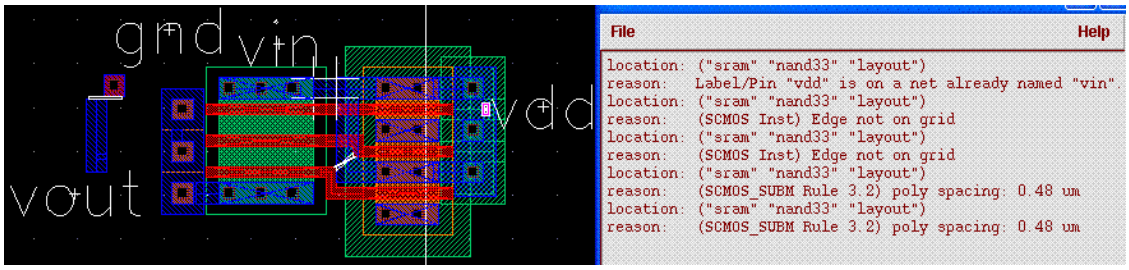
Paramters

Cw = 12.60438 fF
Cw1 = 1.8641f
SRAM pitch = 1.92um
Inverter-inverter-nand-not-nand-not widths
pwidth = 0.7200 2.64 1.5 5.4 1.44 5.34
nwidth = 0.3600 1.32 2.22 2.7 2.16 2.64

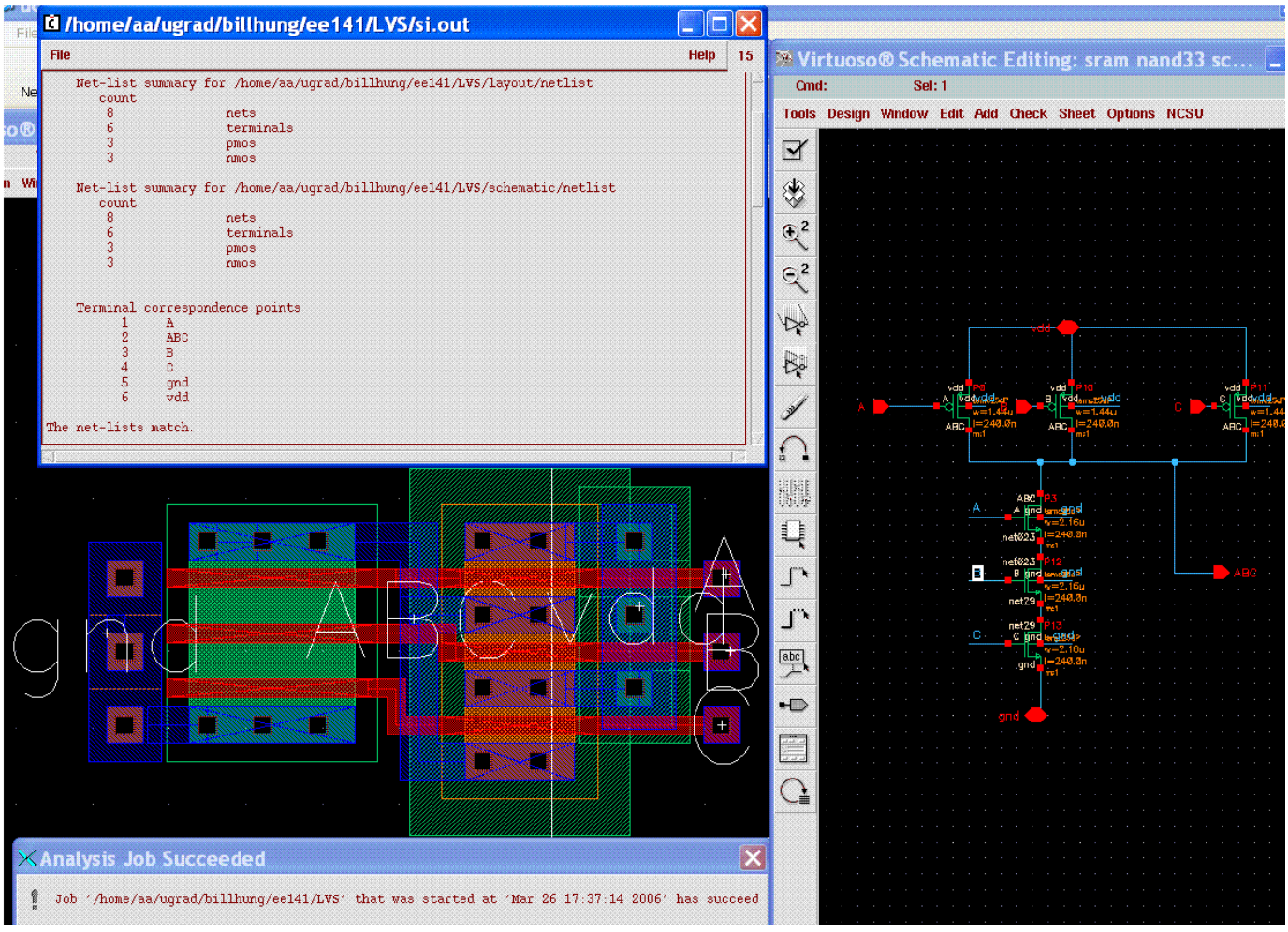
Cadence Layout

Postcoder

NAND



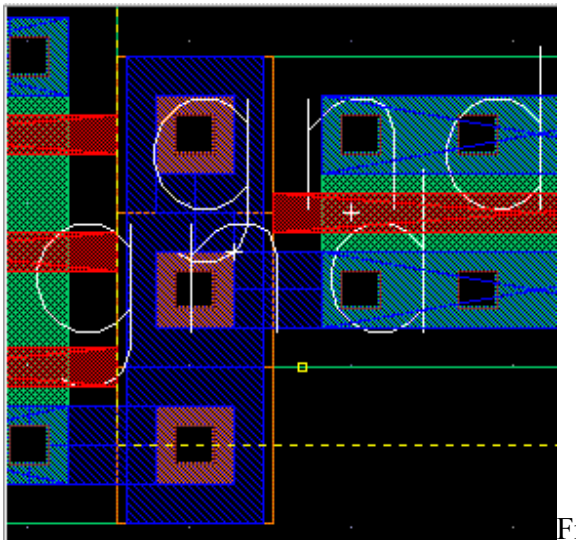
After moving the two poly apart, deleting vdd, and the metal-1 wire, everything is fine again.



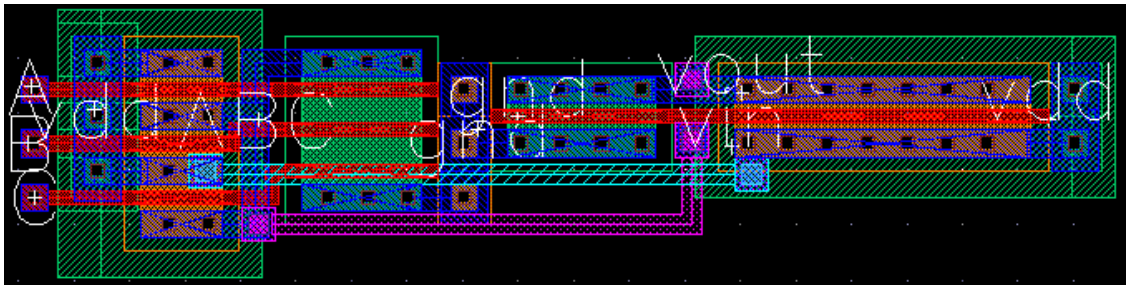
Final layout passes the LVS. Note that the inputs were tricky while trying to keep the nand in 2 pitches. Neither I have enough space to put poly-M1 contacts around the drain or source of NMOS, nor am I allowed to extend inputs to poly gates to ground. Fortunately, there are spaces between the NTAPs, so I am able to extend the gates there

Postdecoder

Postdecoder is between the predecoder and the memory array. Postdecoder is consisted of the one 3-input nand followed by an inverter. The difficult part is that we need to make the pitch of 3-input nand the same as the pitch of the memory cell. After several tries and ideas, we decided to use 2 pitches instead of 1 pitch.



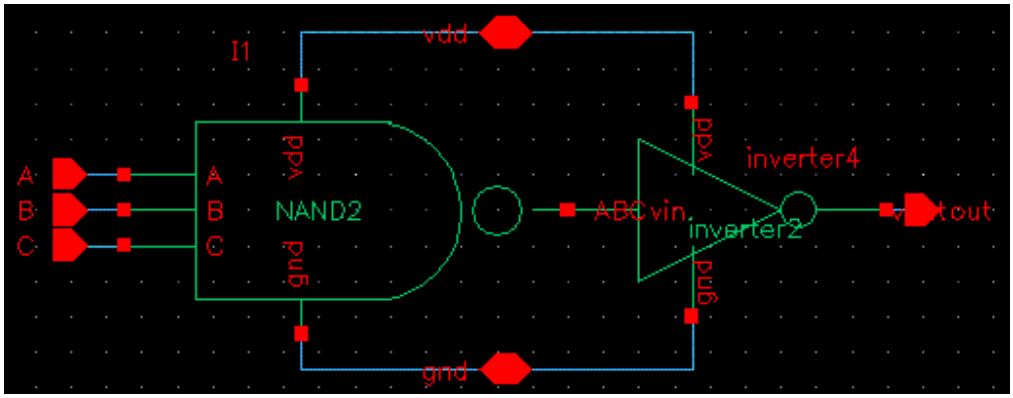
First, I changed the layout of both inverter4 and nand33; M1_P is not filled with M1 completely now. This way, I am able to overlap the ground. Otherwise, I will get DRC error saying that M1 is too close to active



Connect the output of 3-input nand and the input of the inverter, wire vdd node together, and extend the n well of nand. It is DRC free.

Cadence schematic

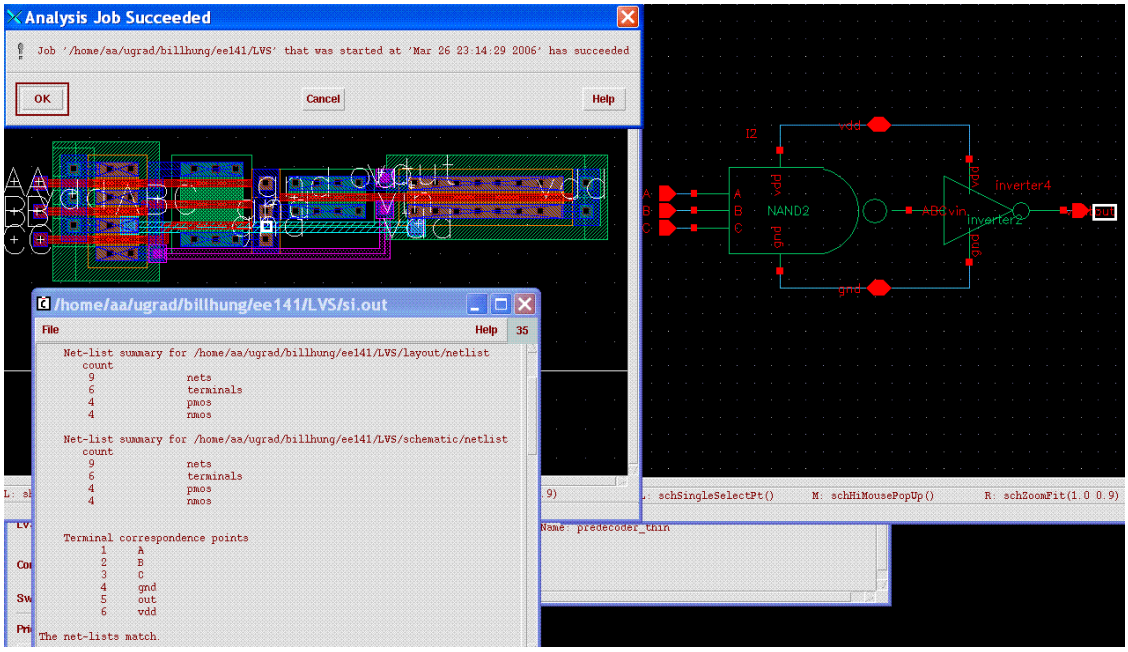
Postdecoder



Connect the nand and inverter as shown above.

```
   Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist
      count
       9               nets
       6               terminals
       4               pmos
       4               nmos

   Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist
      count
       9               nets
       6               terminals
       4               pmos
       4               nmos


   Terminal correspondence points
         1     A
         2     B
         3     C
         4     gnd
         5     out
         6     vdd

   Ill-defined correspondence points.

       N11     N11  Purged because neither is a subset of the other

The net-lists failed to match.

                            layout  schematic
                               instances
       un-matched              0       0
       rewired                 3       0
       size errors             0       0
       pruned                  0       0
       active                  8       8
       total                   8       8

                                 nets
       un-matched              2       2
       merged                  0       0
       pruned                  0       0
       active                  9       9
       total                   9       9
```

However, it doesn't pass the LVS. The reason was that I connected the ground incorrectly.



After fixing it, it is now DRC and LVS free.

Netlist extraction

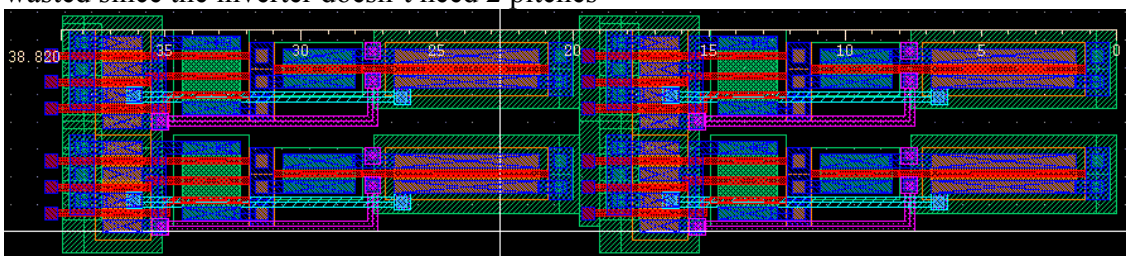
The circuit is what we expected. The wire connections are correct, and the W/L are correct as well. But the pin names are not displayed

```
* # FILE NAME: /HOME/AA/UGRAD/BILLHUNG/CADENCE/SIMULATION/POSTDECODER/
* HSPICES/EXTRACTED/NETLIST/POSTDECODER.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON MAR 26 23:24:37 2006

M0 4 6 5 5 TSMC25DP L=240E-9 W=1.44E-6 AD=864.000006522286E-15
+AS=518.39999307135E-15 PD=2.64000004790432E-6 PS=720.000002729648E-9
M=1
M1 5 7 4 5 TSMC25DP L=240E-9 W=1.44E-6 AD=518.39999307135E-15
+AS=518.39999307135E-15 PD=720.000002729648E-9 PS=720.000002729648E-9
M=1
M2 4 3 5 5 TSMC25DP L=240E-9 W=1.44E-6 AD=518.39999307135E-15
+AS=864.000006522286E-15 PD=720.000002729648E-9 PS=2.64000004790432E-6
M=1
M3 5 4 9 5 TSMC25DP L=240E-9 W=5.34E-6 AD=3.20399999934051E-12
+AS=3.20399999934051E-12 PD=6.53999995847698E-6 PS=6.53999995847698E-6
M=1
M4 2 6 8 2 TSMC25DN L=240E-9 W=2.16E-6 AD=1.29599998267838E-12
+AS=518.39999307135E-15 PD=3.35999993694713E-6 PS=479.999982871959E-9
M=1
M5 8 7 1 2 TSMC25DN L=240E-9 W=2.16E-6 AD=518.39999307135E-15
+AS=518.39999307135E-15 PD=479.999982871959E-9 PS=479.999982871959E-9
M=1
M6 1 3 4 2 TSMC25DN L=240E-9 W=2.16E-6 AD=518.39999307135E-15
+AS=1.29599998267838E-12 PD=479.999982871959E-9 PS=3.35999993694713E-6
M=1
M7 2 4 9 2 TSMC25DN L=240E-9 W=2.64E-6 AD=1.58399996678243E-12
+AS=1.58399996678243E-12 PD=3.83999986297567E-6 PS=3.83999986297567E-6
M=1
* INCLUDE FILES
```

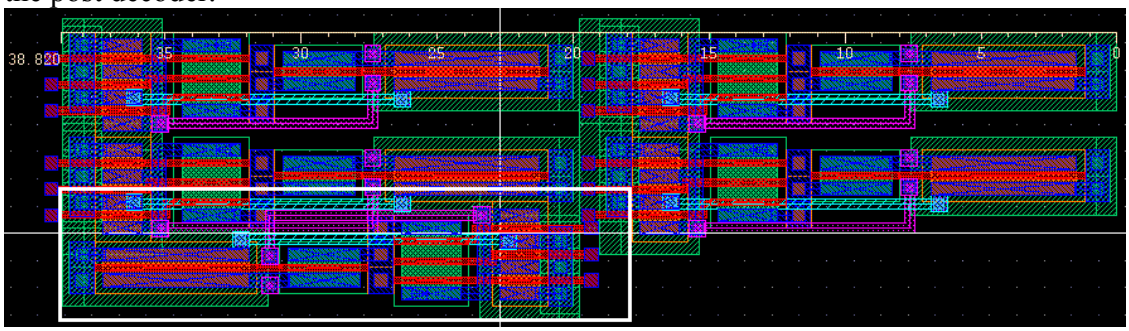
```
* END OF NETLIST
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
.END
```

Example of Sharing Pitches

Since the post-decoder occupies 2 pitches, we have to put the other post-decoder on the side; therefore, the post-decoder grows longer. As we can see, there are still some spaces wasted since the inverter doesn't need 2 pitches



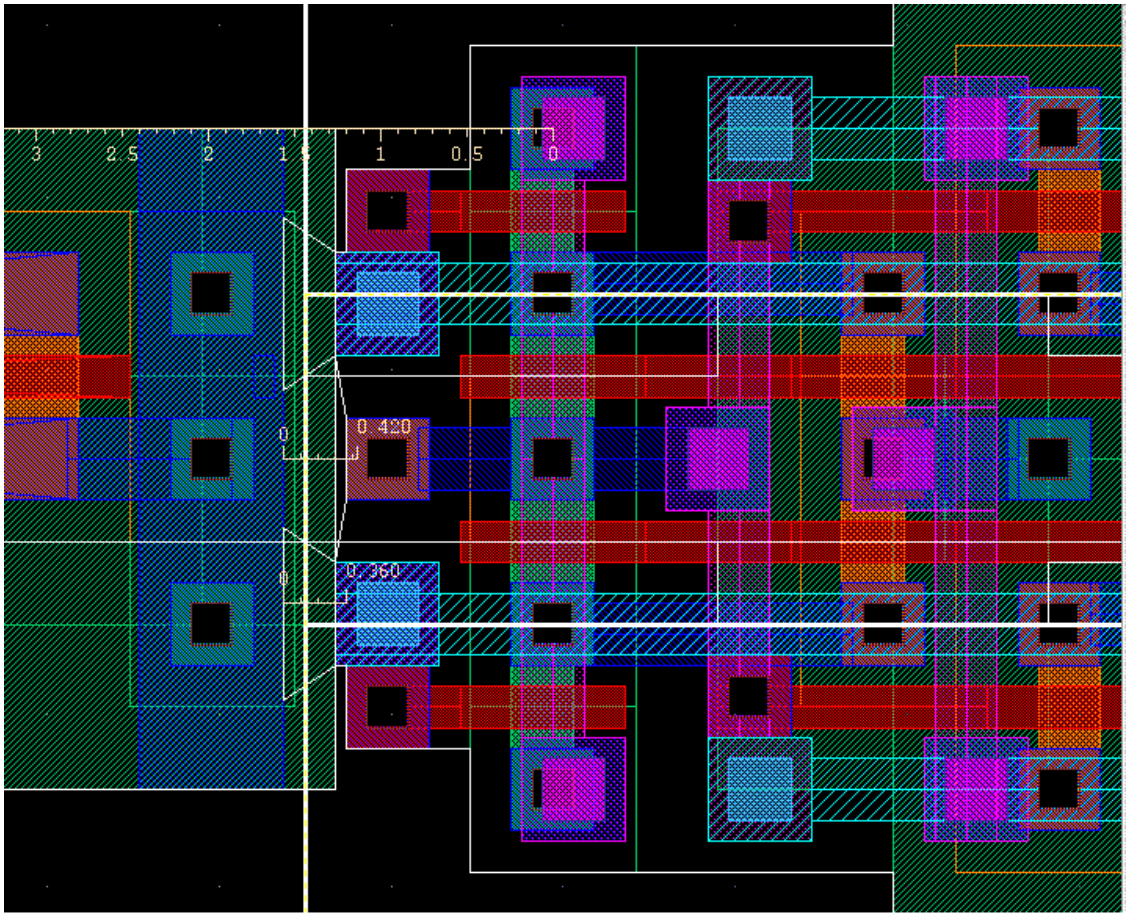
I was thinking maybe we could flip the neighbor the other way around (below), but I doubt that it will work, and the wiring might be complicated. So we decided not to flip the post decoder.



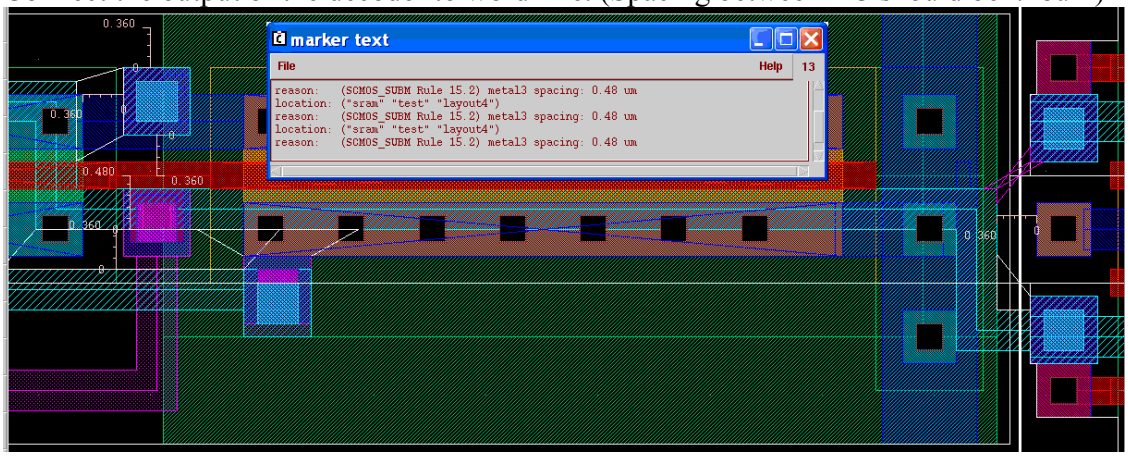
Connecting Post-decoder and a memory array

Extending the n well of the inverter of the post-decoder, and supply rails (including vdd and gnd) to 2 pitches so that Cadence will not complain about different well potentials or different supply rails

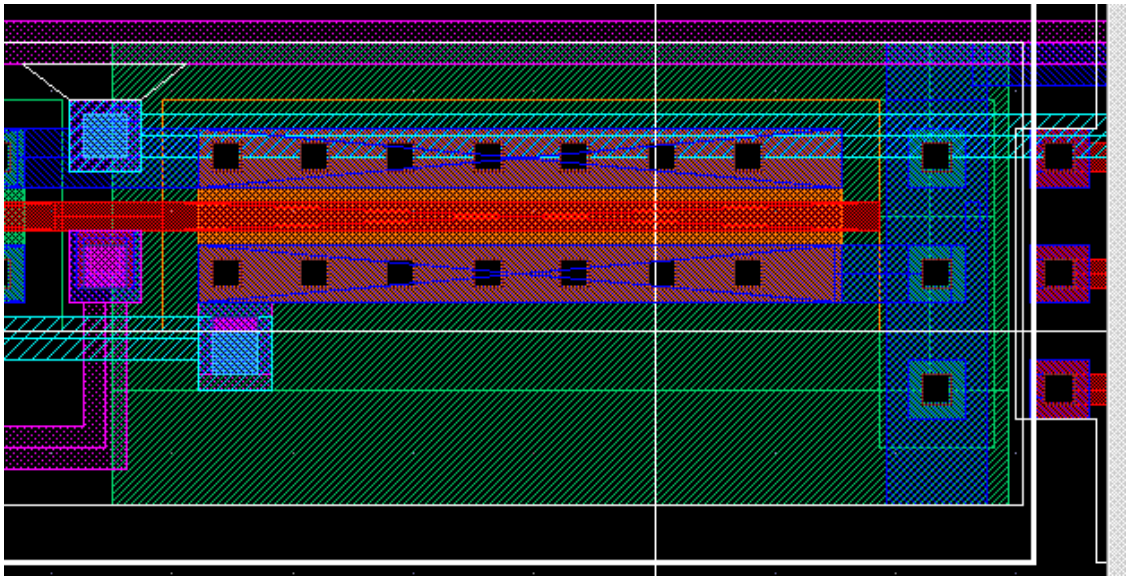
Next, try to connect the memory cell and the post decoder together. The figure below showed that active region should be at least 0.36um from the n well.



Connect the output of the decoder to word line. (Spacing between M3 should be .48um)



Spacing between M2 and M2_M3 is also 0.48um



Circuit Extraction

```
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03       '
.TITLE '* # file name:
/home/aa/ugrad/billhung/cadence/simulation/decoder/hspi'
 tplh             tphl             trise            tfall
 temper           alter#
  1.827e-10        1.271e-10        1.784e-10        1.175e-10
   25.0000          1.0000
```

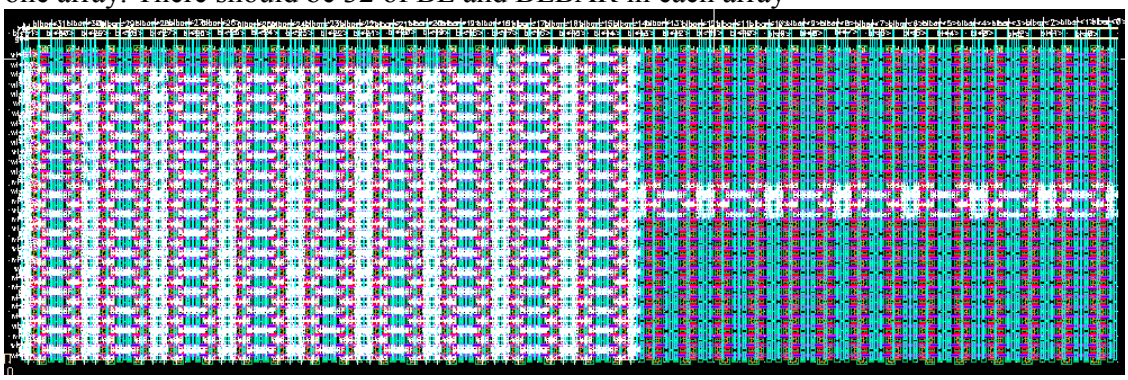
Original Simulation vs Extracted
(The original circuit simulation and extracted netlist are inside the Keep folder. Note that the worst case is when all the inputs to nand are changing at the same time)
It turns out that the extracted netlist is very close to what we simulated originally

Original netlist with all the inputs to nand changing at the same time

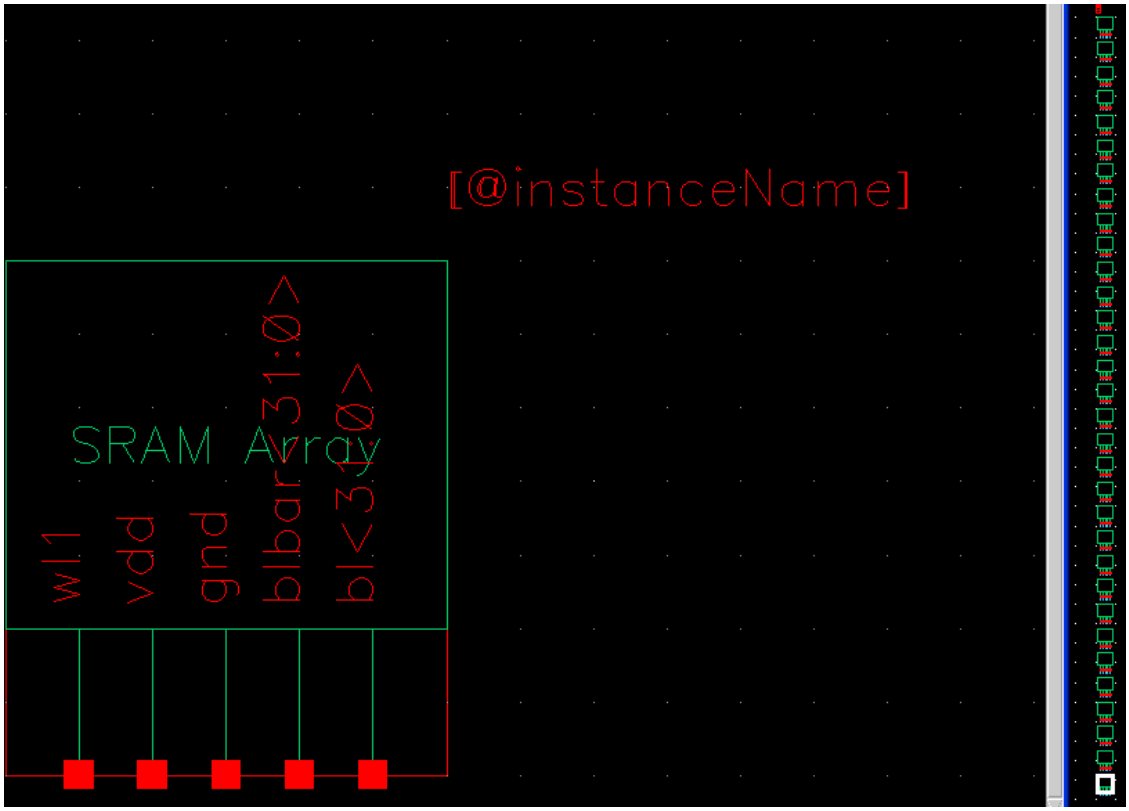
```
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03       '
.TITLE '*** phase ii'
 tplh             tphl             trise            tfall
 tp               temper           alter#
  9.639e-10        7.131e-10        1.980e-10        1.189e-10
  8.385e-10        25.0000          1.0000
```

32 x 32 sram

Adding pins on each word line, also note that BL and BLBAR are not connected within one array. There should be 32 of BL and BLBAR in each array



Changing the schematic so that it is easier to wire



LVS passed
@(#)$CDS: LVS version 5.0.0 12/19/2003 23:46 (cds12107) $

Command line: /usr/eesww/cadence/current/IC5.0.33/tools.sun4v/dfII/bin/32bit/LVS -dir /home/aa/ugrad/billhung/ee141/LVS -l -s -t /home/aa/ugrad/billhung/ee141/LVS/layout /home/aa/ugrad/billhung/ee141/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/layout/netlist
count
2146 nets
98 terminals
2048 pmos
4096 nmos

Net-list summary for /home/aa/ugrad/billhung/ee141/LVS/schematic/netlist
count
2146 nets
98 terminals
2048 pmos

4096 nmos

Terminal correspondence points

1	bl<0>
2	bl<10>
3	bl<11>
4	bl<12>
5	bl<13>
6	bl<14>
7	bl<15>
8	bl<16>
9	bl<17>
10	bl<18>
11	bl<19>
12	bl<1>
13	bl<20>
14	bl<21>
15	bl<22>
16	bl<23>
17	bl<24>
18	bl<25>
19	bl<26>
20	bl<27>
21	bl<28>
22	bl<29>
23	bl<2>
24	bl<30>
25	bl<31>
26	bl<3>
27	bl<4>
28	bl<5>
29	bl<6>
30	bl<7>
31	bl<8>
32	bl<9>
33	blbar<0>
34	blbar<10>
35	blbar<11>
36	blbar<12>
37	blbar<13>
38	blbar<14>
39	blbar<15>
40	blbar<16>
41	blbar<17>

42 blbar<18>
43 blbar<19>
44 blbar<1>
45 blbar<20>
46 blbar<21>
47 blbar<22>
48 blbar<23>
49 blbar<24>
50 blbar<25>
51 blbar<26>
52 blbar<27>
53 blbar<28>
54 blbar<29>
55 blbar<2>
56 blbar<30>
57 blbar<31>
58 blbar<3>
59 blbar<4>
60 blbar<5>
61 blbar<6>
62 blbar<7>
63 blbar<8>
64 blbar<9>
65 gnd
66 vdd
67 wl<0>
68 wl<10>
69 wl<11>
70 wl<12>
71 wl<13>
72 wl<14>
73 wl<15>
74 wl<16>
75 wl<17>
76 wl<18>
77 wl<19>
78 wl<1>
79 wl<20>
80 wl<21>
81 wl<22>
82 wl<23>
83 wl<24>
84 wl<25>
85 wl<26>
86 wl<27>

87	wl<28>
88	wl<29>
89	wl<2>
90	wl<30>
91	wl<31>
92	wl<3>
93	wl<4>
94	wl<5>
95	wl<6>
96	wl<7>
97	wl<8>
98	wl<9>

The net-lists match.

	layout	schematic	
	instances		
un-matched	0	0	
rewired		0	0
size errors	0	0	
pruned	0	0	
active	6144	6144	
total	6144	6144	
	nets		
un-matched	0	0	
merged	0	0	
pruned	0	0	
active	2146	2146	
total	2146	2146	
	terminals		
un-matched	0	0	
matched but different type	0	0	
total	98	98	

Probe files from /home/aa/ugrad/billhung/ee141/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/aa/ugrad/billhung/ee141/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

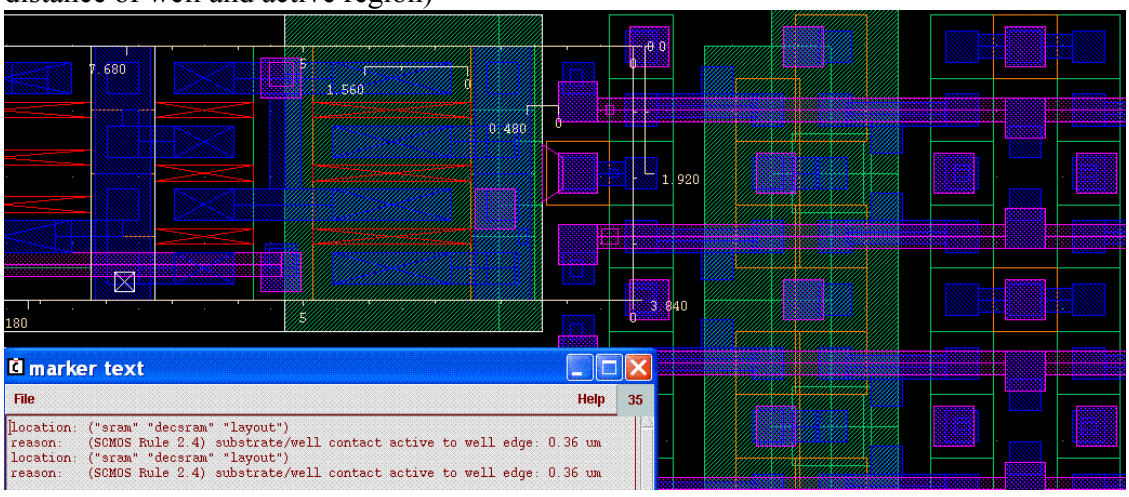
prunenet.out:

prunedev.out:

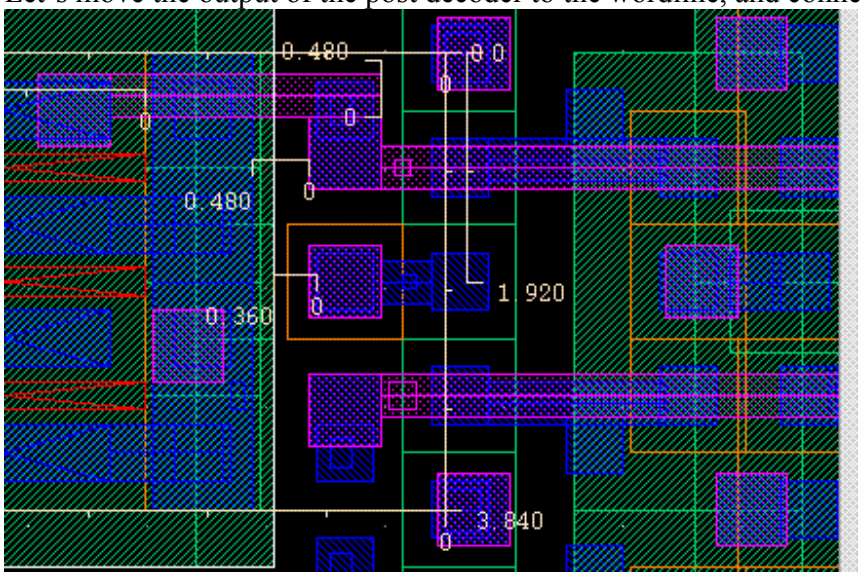
audit.out:

Connecting 32 post decoder to 32 sram arrarys

The shortest distance between post decoder and a SRAM array is 0.36um (limited by the distance of well and active region)

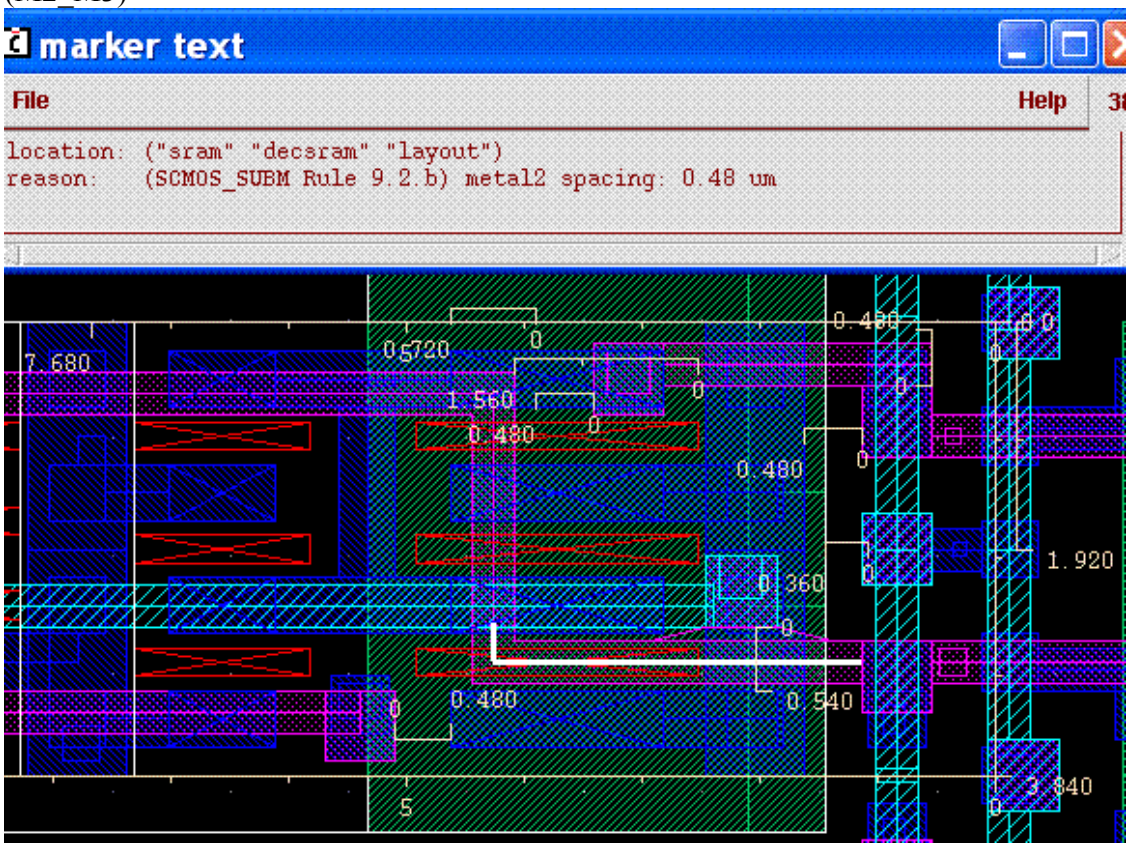


Let's move the output of the post decoder to the wordline, and connect the wordline



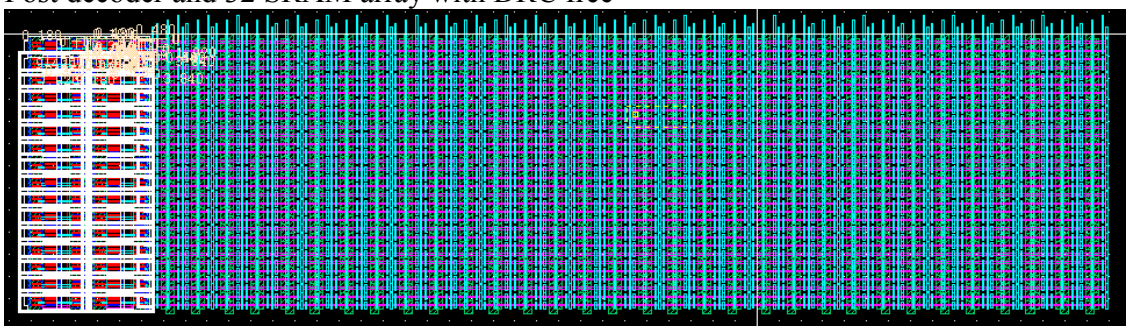
Next put another post decoder on the left of the post decoder. (Note: we need to fill in n well to have the same potential. The closest distance of the post decoder is limited by M1 spacing 0.36um)

The output of the second post decoder (M2) needs to be 0.48um away from Vdd (M2_M3)



CAUTION: This implementation creates extra capacitance at the wordline since the second postdecoder needs a long wire to connect the second wordline, so I would expect the delay will be less than what we expected

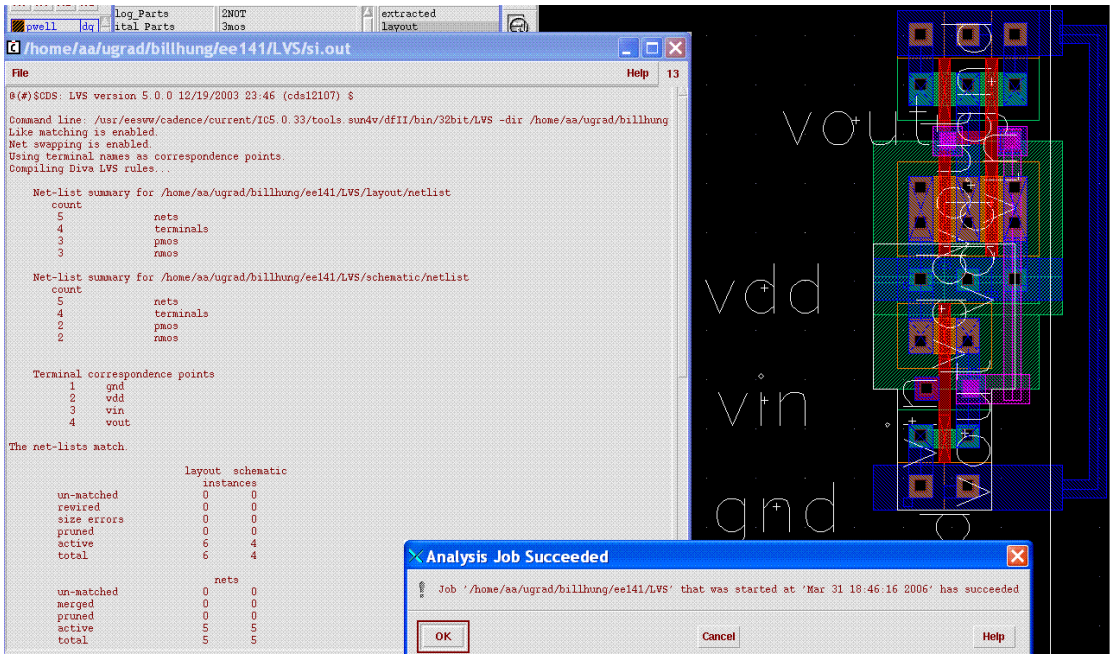
Post decoder and 32 SRAM array with DRC free



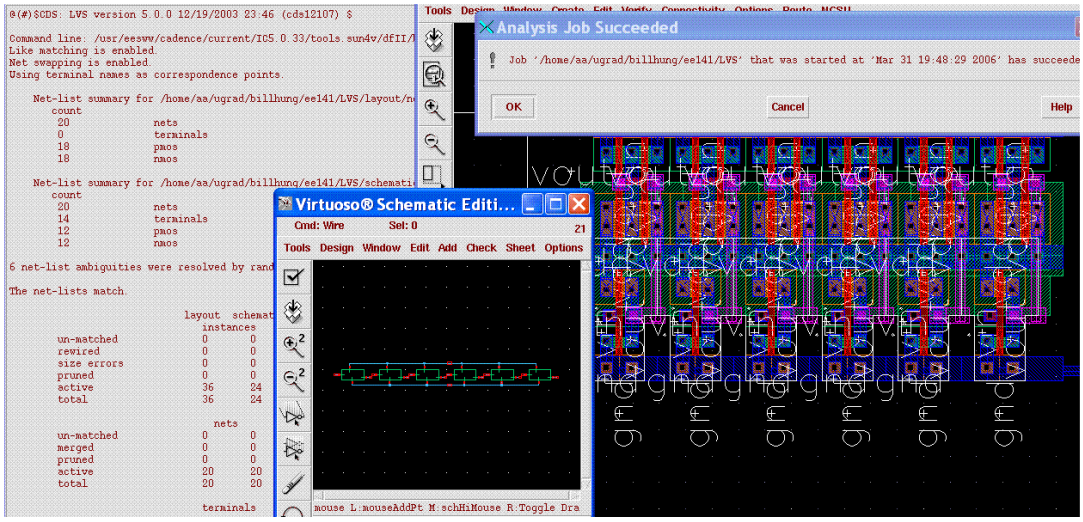
Modify Precoder

Since we need to branch the output of the second inverter, we break the predecoder into 2 gourps. One is the first two inverter, and the other is the 3-input nand and the third inverter

Two inverters

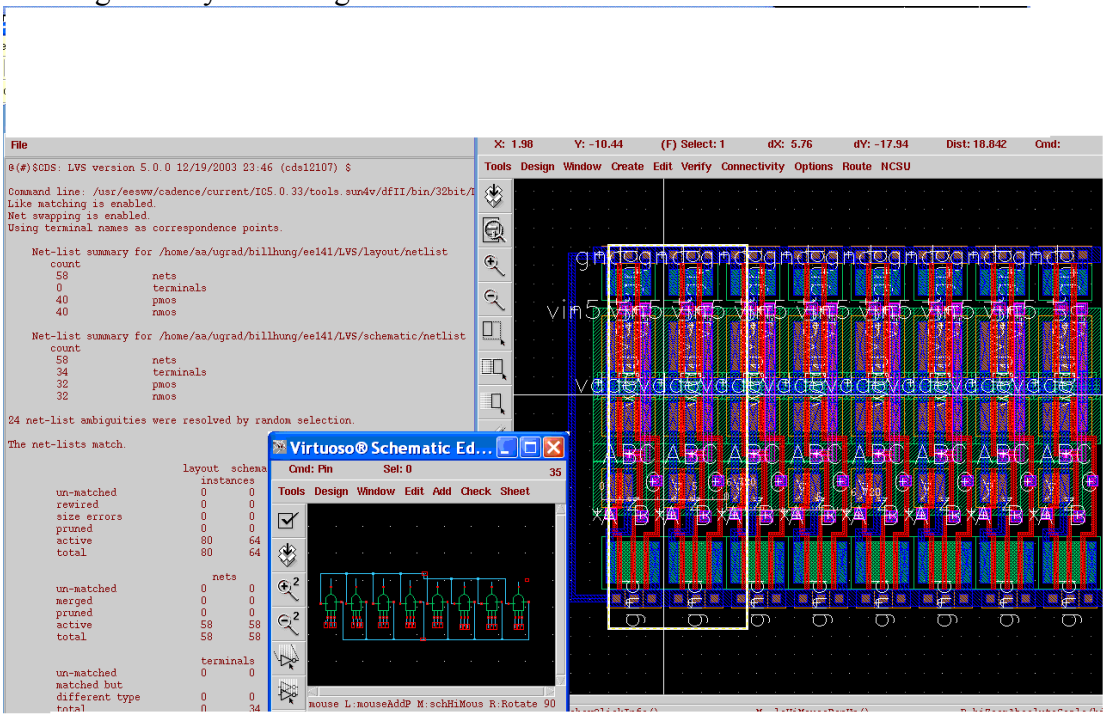


Create an array of 2 inverters



AND

Creating an array of AND gate

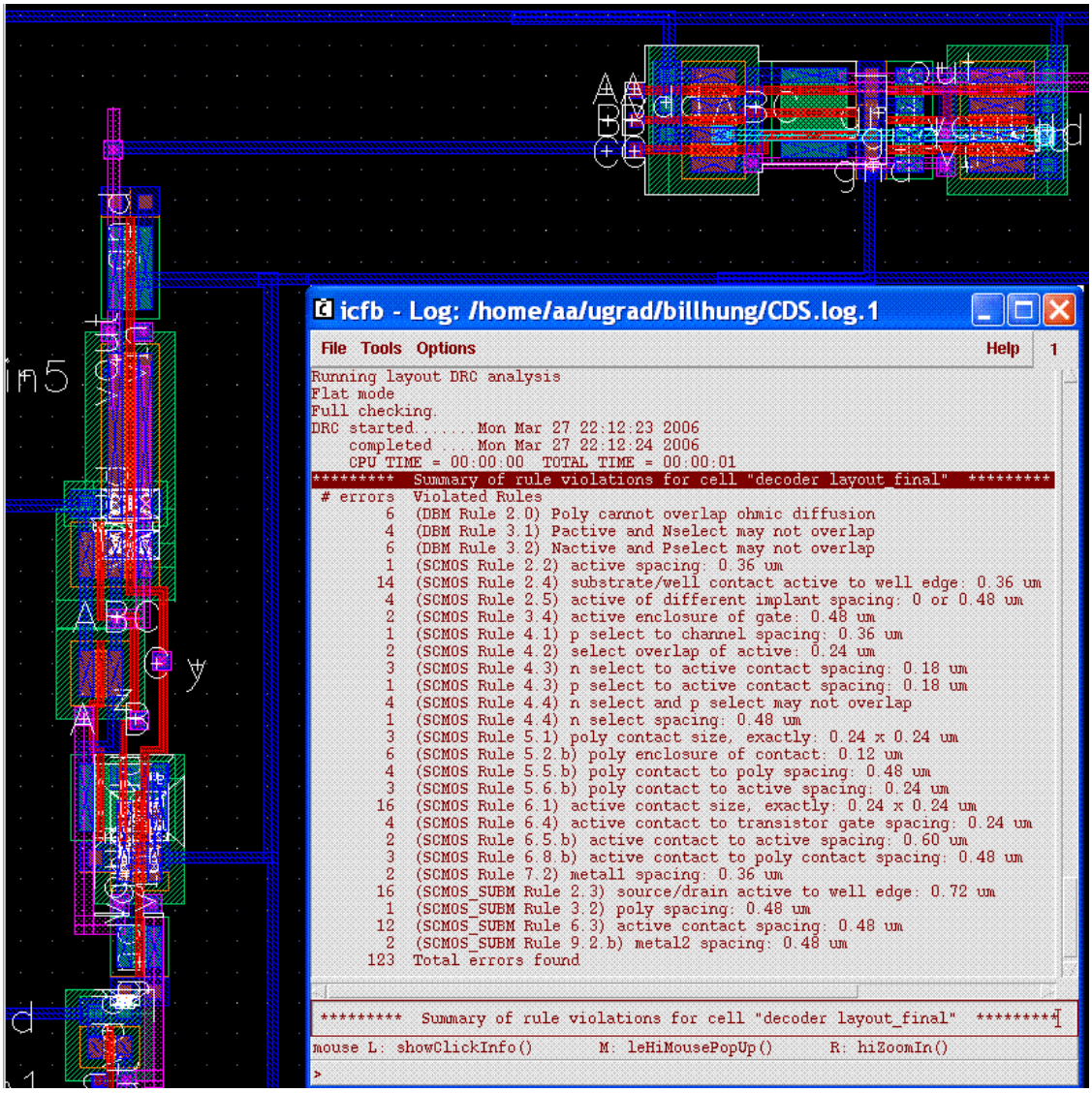


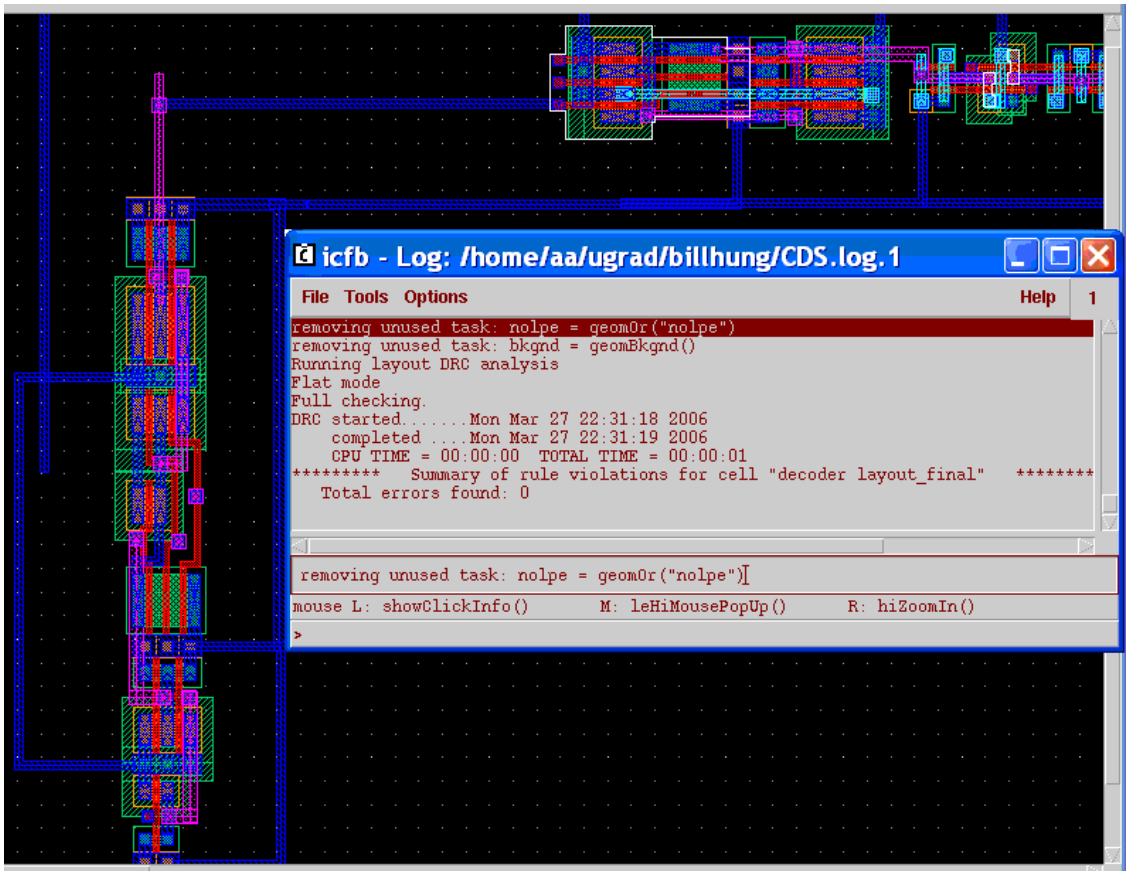
Putting the two together to form predecoder
LVS result

Running simulation in directory: "/home/aa/ugrad/billhung/ee141/LVS".

```
Begin netlist:    Apr  1 12:32:55 2006
        view name list = ("auLvs" "extracted" "schematic")
        stop name list  = ("auLvs")
        library name    = "sram"
        cell name       = "newpredecoder"
        view name       = "extracted"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:    Apr  1 12:32:56 2006

Moving original netlist to extNetlist
Removing parasitic components from netlist
        presistors removed:  0
        pcapacitors removed: 0
        pinductors removed:  0
        pdiodes removed:     0
        trans lines removed: 0
        52 nodes merged into 52 nodes


Begin netlist:    Apr  1 12:32:56 2006
        view name list = ("auLvs" "schematic")
        stop name list  = ("auLvs")
        library name    = "sram"
        cell name       = "newpredecoder"
        view name       = "schematic"
        globals lib     = "basic"
Running Artist Flat Netlisting ...
*WARNING* invalid cell view -- 0(unknown)
*WARNING* invalid cell view -- 0(unknown)
global error:
Cannot find switch master cell for instance I2 in cellView (newpredecoder schematic)
from viewlist 'auLvs schematic ' in library 'sram'.
*WARNING* invalid cell view -- 0(unknown)
        si: Netlist did not complete successfully.
End netlist:    Apr  1 12:32:56 2006


Comparison program did not complete.
```

NG Cadence screenshots




icfb - Log: /home/aa/ugrad/billhung/CDS.log.1
File Tools Options
Help
1
removing unused task: nolpe = geomOr("nolpe")
removing unused task: bkgnd = geomBkgnd()
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Mon Mar 27 22:31:18 2006
completed ....Mon Mar 27 22:31:19 2006
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
********* Summary of rule violations for cell "decoder layout_final" ********
Total errors found: 0
removing unused task: nolpe = geomOr("nolpe")
mouse L: showClickInfo() M: leHiMousePopUp() R: hiZoomIn()
>