UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EECS 141: Digital Integrated Circuits - Spring 2006

Report Cover Sheet

TERM PROJECT: SRAM Design Cover Sheet

Report 1 – Memory cell design
Due Monday, March 20, 2006 by 10am in drop box.

Names
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Parameter	Pre-design estimate	Units
Cell area	13.3632 ($928\lambda^2$)	μm^2
Read noise margin	250	mV
Voltage rise during read	393.6	mV

	GRADE
Approach, result and correctness (60%)	
Report (40%)	
TOTAL	

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SRAM Cell Design

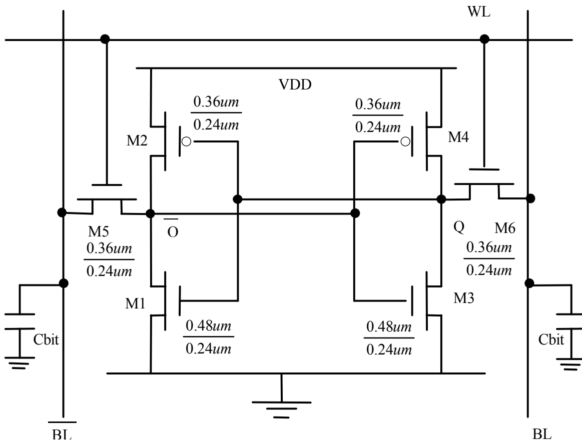

Figure 1: SRAM Cell Schematic

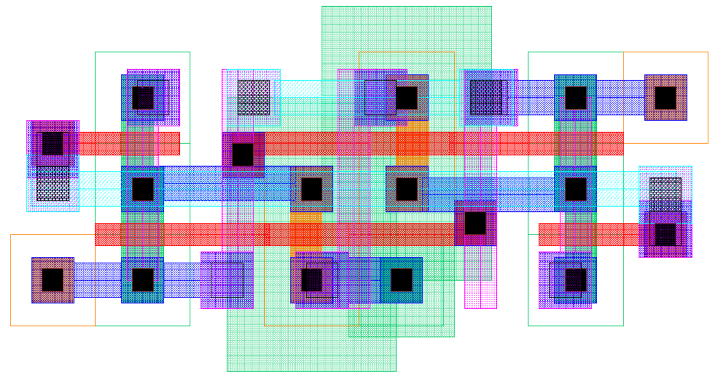

Figure 2: Cadence SRAM Cell Layout

(left) The pull-up transistors and the access transistors are minimum sized (W/L=0.36/0.24) to give a pull-up ratio of 1(<1.5). The pull-down transistors are sized W/L=0.48/0.24 to meet the 0.4V read margin. The cell ratio is 1.33(>1.2). (right) The goal of the layout is to make it work with minimum size.

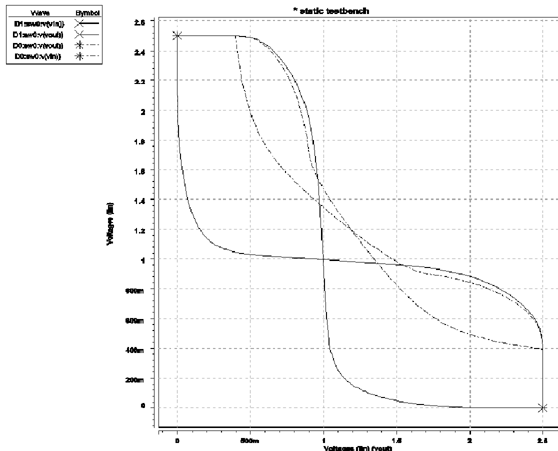

Figure 3: HSPICE Static Noise Margin

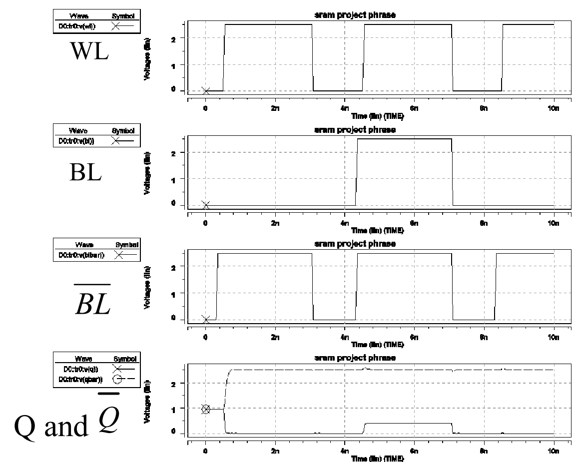

Figure 4: HSPICE Read and Write Simulation

(left) Voltage Transfer Curve (VTC) of an inverter and a half cell taken from the SRAM cell. The read margin of 0.4V is met. Note that the two axises are in different scale. (right) A write simulation wrote a zero into the SRAM cell, followed by a read simulation shows the read margin is below 0.4V. Note that when the word line is low initially, Q and $\overline{Q}$ have don't care values

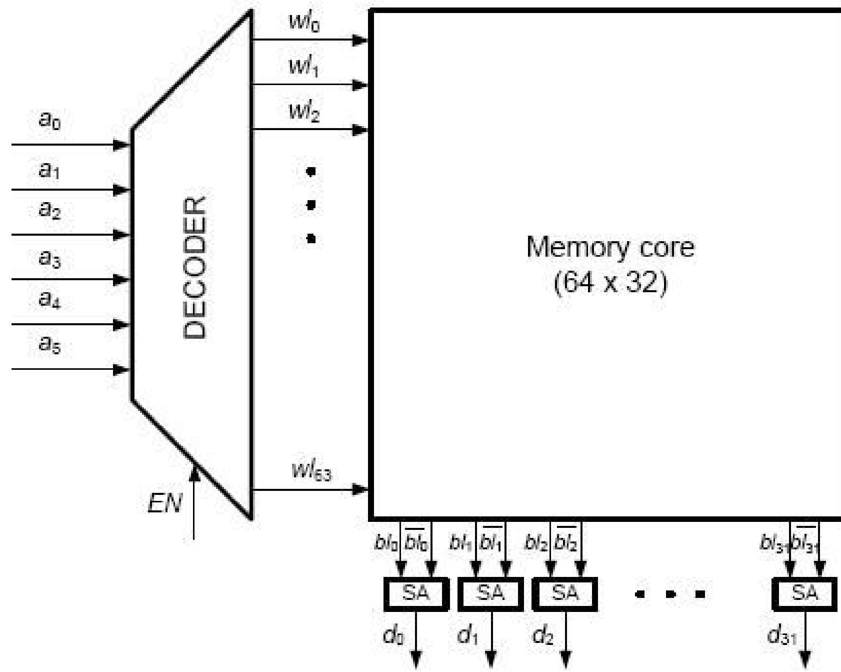

Figure 1 High Level SRAM array block diagram

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PHRASE I Minimize a SRAM Cell

The phrase I involes minimizing a SRAM area, stimulating the SRAM design with HSPICE. and drawing the layout for the minimum sized SRAM using Cadence.

Figure 2 SRAM Schematic

Sizing Methodology

Pull Up Transistors

The two pull up transistors (M2 and M4) in Figure 2 are minimum sized. Because the Pull Up ratio between the pull up transistors and the access transistors equals to 1 if they are all minimum sized. The pull-up ratio needs to be less than 1.8 [Rabaey, 661]. From Cadence, the minimum size is when W=0.36um, and L=0.24um.

$$PR = \frac{W_4 / L_4}{W_6 / L_6}$$

Equation 1:Pull-up Ratio [Rabaey, 661]

Access Transistors

The two access transistors (M5 and M6) in Figure 2 are minimum sized. Practical designs sometimes increase the length (L) of these access transistors to improve the robustness of

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the SRAM design. Larger L can give less leakage because of longer channel length, but it adds more load to the bit line. In this design, the L of the access transistors are at their minimum lengths. In order to compensate for the minimum lenghts of the access transistors, the width (W) of the pull down transistors are increased.

Pull Down Transistors

The width of the pull down transistors (M1 and M3) is the main parameter to optimize. The goal of the minimizing is to make sure "the SRAM still works" as expected. The critical point to meet the specification to have ΔV of $\overline{Q}$ below 0.4V. That is :

$\Delta V(\overline{Q}) < 0.4V$. According to the equation

$$CR = \frac{W_1 / L_1}{W_5 / L_5}$$ Equation 2:Cell Ratio [Rabaey, 659]

where CR is called t he cell ratio [Rabaey, 659]

CR is about 1.2[Rabaey, 659]. So

$$CR = \frac{W_1 / L_1}{W_5 / L_5} = \frac{W_1}{W_5} = 1.2$$
$$W_1 = 1.2 \cdot W_5$$

If W_5 is minimum sized, W_1 is 1.2 times the minimum size. As HW3#3a suggested, the minimum NMOS has L=0.24um, and W=0.36um. So,

$$W_1 = 1.2 \cdot (0.36um) = 0.432um$$

However, with W1 = 0.432um, the read margin exceed the 0.4V specification.

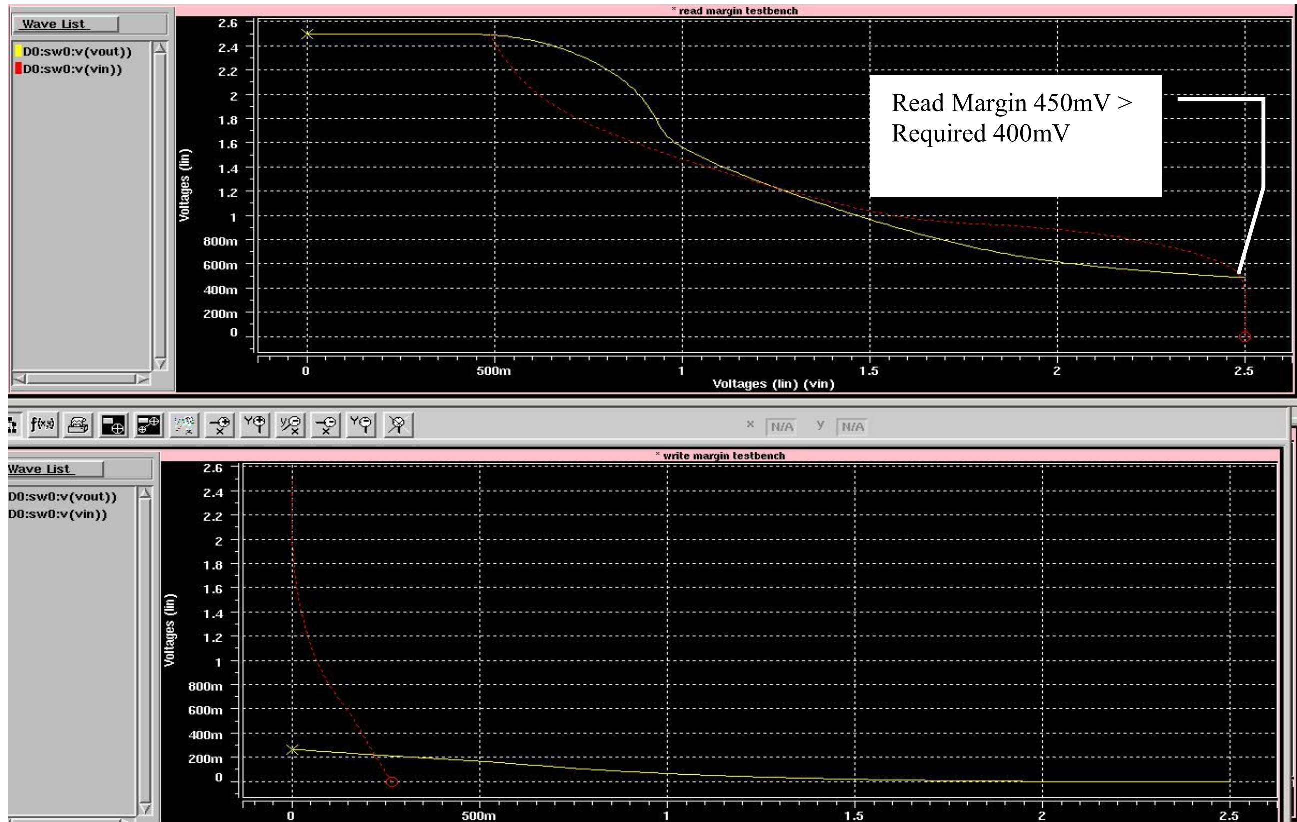


Figure 3 Read margin and Write margin with W_1 = 0.432um. Read Margin is 450mV, which is larger than the required 400mV.

Therefore, we increased the width to 0.48um, CR = 1.33, which will gives a read margin 0.3936. A read margin of 0.3936V is better than the required read margin 0.4V.Also note that the width needs to be multiple of lambda in the layout, 0.12um. At this point, both read margin and write margin are below 0.4V. Note that we could increase the width even further to lower the read margin, but since our goal is to minize the size, we used 0.48um.

Read Operation

The read margin has to be met. The read margin is designed so that $\overline{Q}$ does not exceed 0.4V during a read operation.

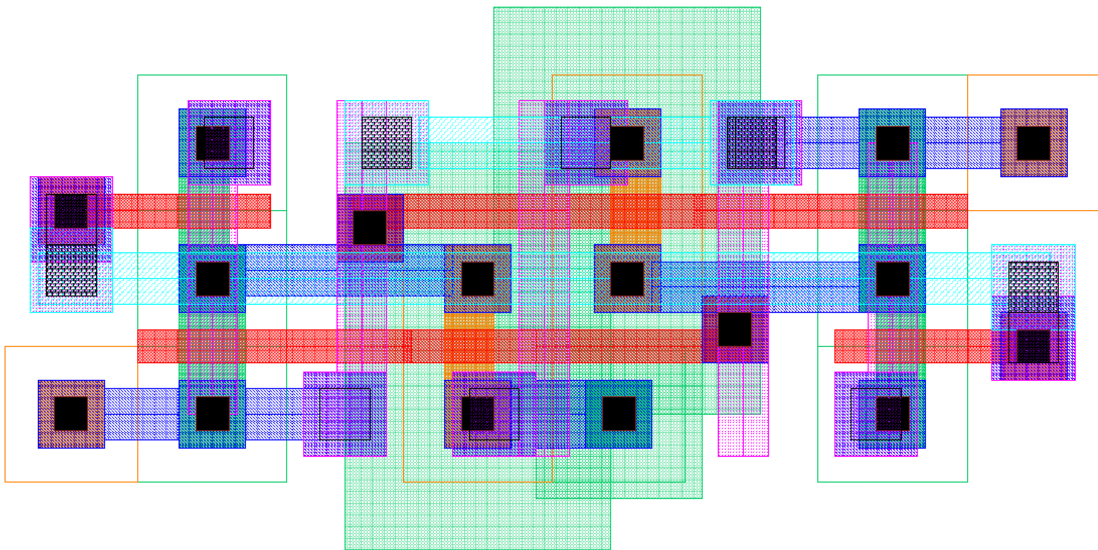
Write Operation

This project needs to meet the write margin. According to Professor Nikolic, the write margin is "the highest voltag on BL/$\overline{BL}$ that writes a zero into the cell".

HSPICE Stimulation

As we increase the width of the pulldown nmos transistors, the read margin decreases.

Cadence Layout



Phase I Summary

Horizontal Length = 7.2um
Vertical Height = 2.16um
Area = 15.552 um^2 = $1080\lambda^2$

Hours = 39 hours

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Glossary

Area
: The smallest rectangle enclosing the repetitive pattern. In this case, from a contact of one side to the contact of another side.

Read Margin
: is designed so that $\overline{Q}$ does not exceed 0.4V during a read operation.

SRAM
: Static Random Access Memory

Write Margin
: is “the highest voltag on BL/ $\overline{BL}$ that writes a zero into the cell

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Static Noise Margin HSPICE with Pulldown Transistor Width of 1.2*0.36

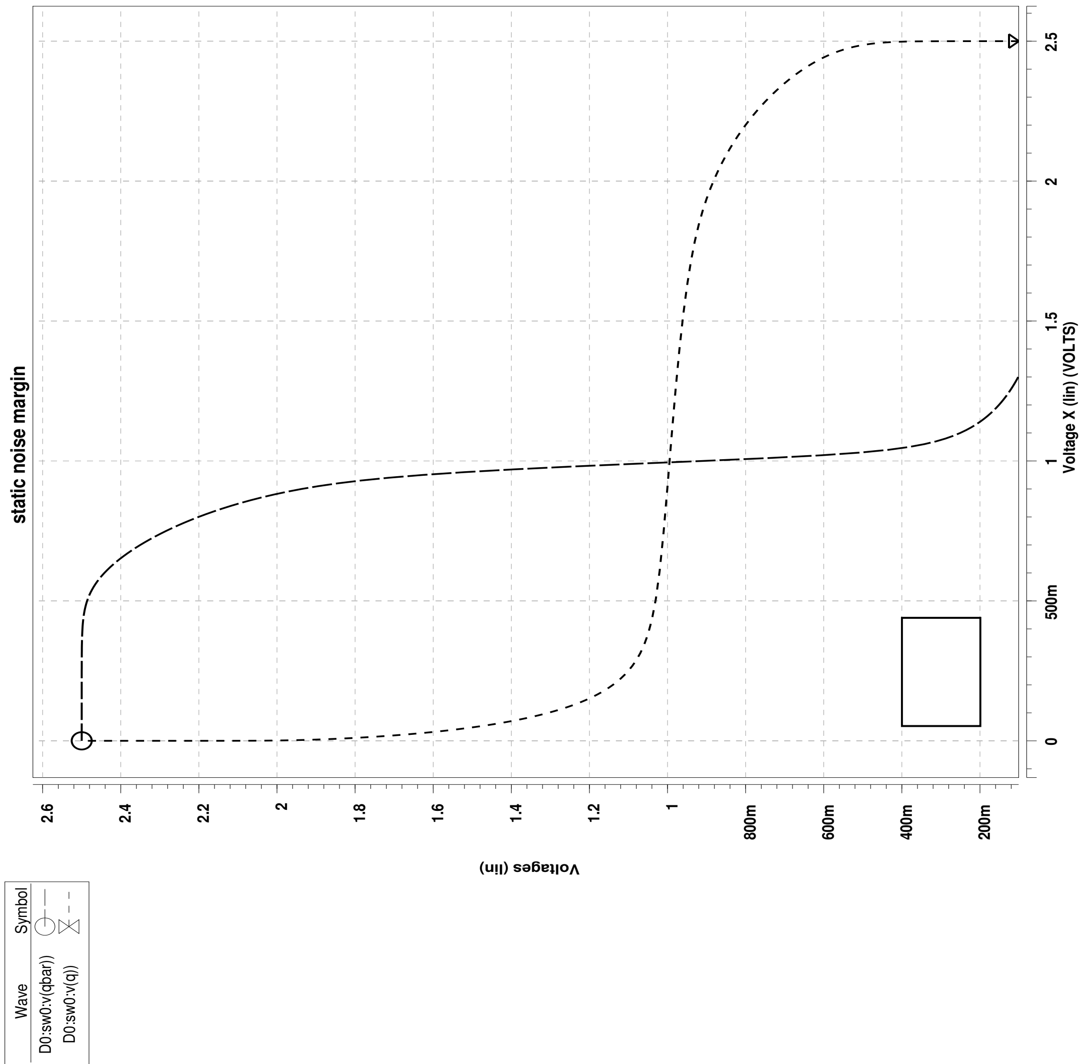

Figure 4 Static Noise Margin VTC HSPICE Plot

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```
Static Noise Margin


.lib '/home/ff/ee141/MODELS/g25.mod' TT

*****************************************
* Parameter
*****************************************
.param vddp=2.5
.param wpulldown=0.36u*1.2
.param pmoswidth=0.36u

*****************************************
* Netlist
*****************************************
VDD vdd 0 'vddp'
vq q 0 2.5V

*M<name> <drain> <gate> <source> <bulk> <model> <geometry>

M1 qbar q 0 0       nmos l=0.24u w='wpulldown'
M2 qbar q vdd vdd  pmos l=0.24u w='pmoswidth'


*****************************************
* Analysis
*****************************************
*nomod= no model info from library
.options post=2 nomod

*.op makes hspice determines DC operating point
.op

.dc vq 0 2.5 0.01

.end
```

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Read Margin HSPICE Simulation

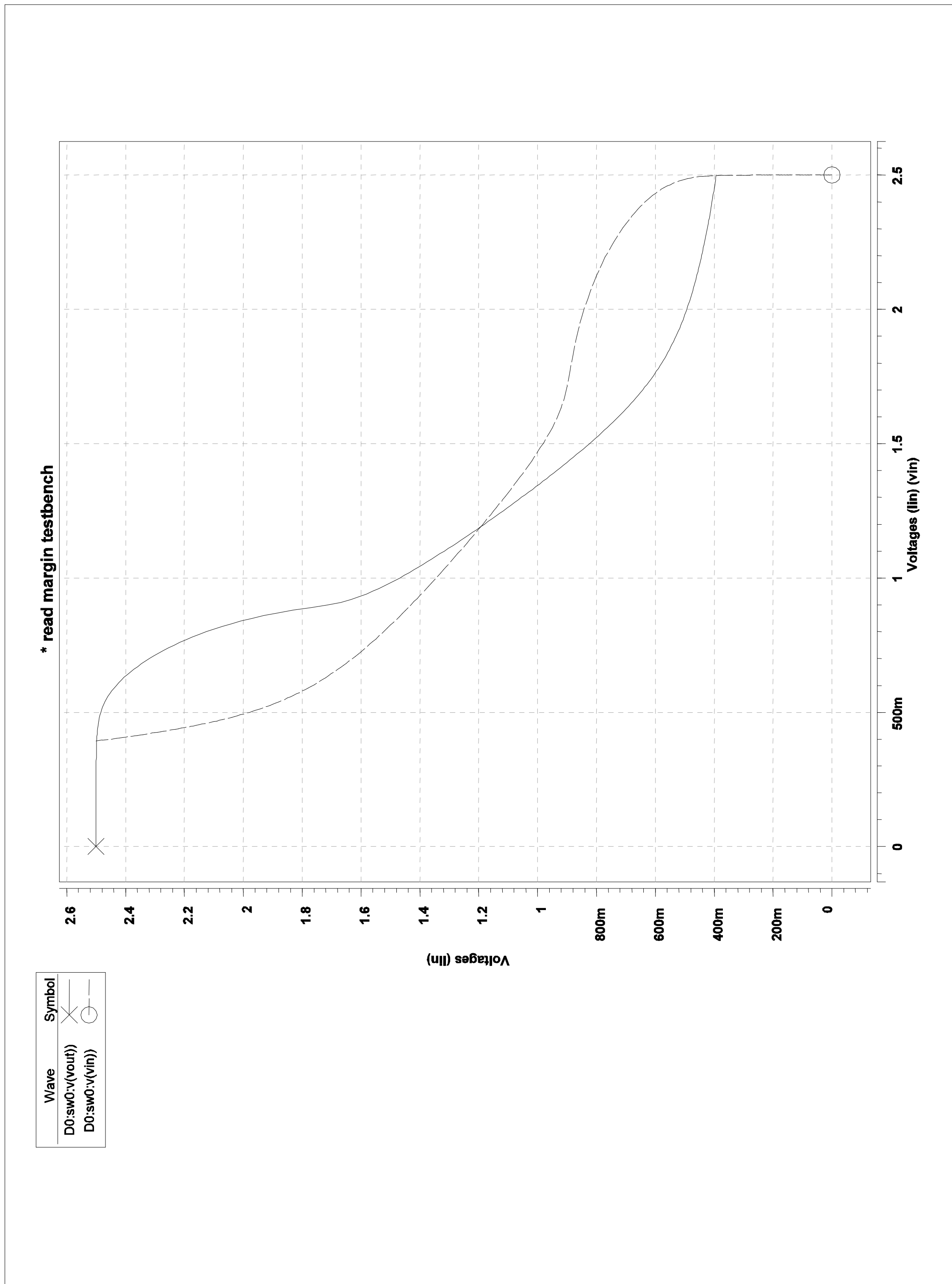

Figure 5 Read margin VTC

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```
** inverter subcircuit
.subckt my_inv vin vout vdd vss
.param wpulldown='0.48u'
.param pmoswidth=0.36u
M1 vout vin vss vss  nmos l=0.24u w='wpulldown'
M2 vout vin vdd vdd  pmos l=0.24u w='pmoswidth'
.ends
```

```
* read margin testbench
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'circuit.sp'
Vdd vdd 0 2.5
Vin VIN 0 dc 2.5
xinv Vin Vout vdd 0 my_inv
M5 vblbar vdd Vout 0 nmos l=0.24u w=0.36u
Vblbar vblbar 0 2.5
.dc Vin 0 2.5 0.01
.option post
.END
```

```
$DATA1 SOURCE='HSPICE' VERSION='V-2004.03       '
.TITLE 'sram project phrase'
 q_max_rd         q_max_wr         temper           alter#
  1.886e-02          0.3936          25.0000           1.0000
```

```
* Write margin testbench (not required for the report)
.lib '/home/ff/ee141/MODELS/g25.mod' TT
.inc  'circuit.sp'
Vdd vdd 0 2.5
Vin VIN 0 dc 2.5
xinv Vin Vout vdd 0 my_inv
M6 vbl vdd Vout 0 nmos l=0.24u w=0.36u
Vbl vbl 0 0
.dc Vin 0 2.5 0.01
.option post
.END
```

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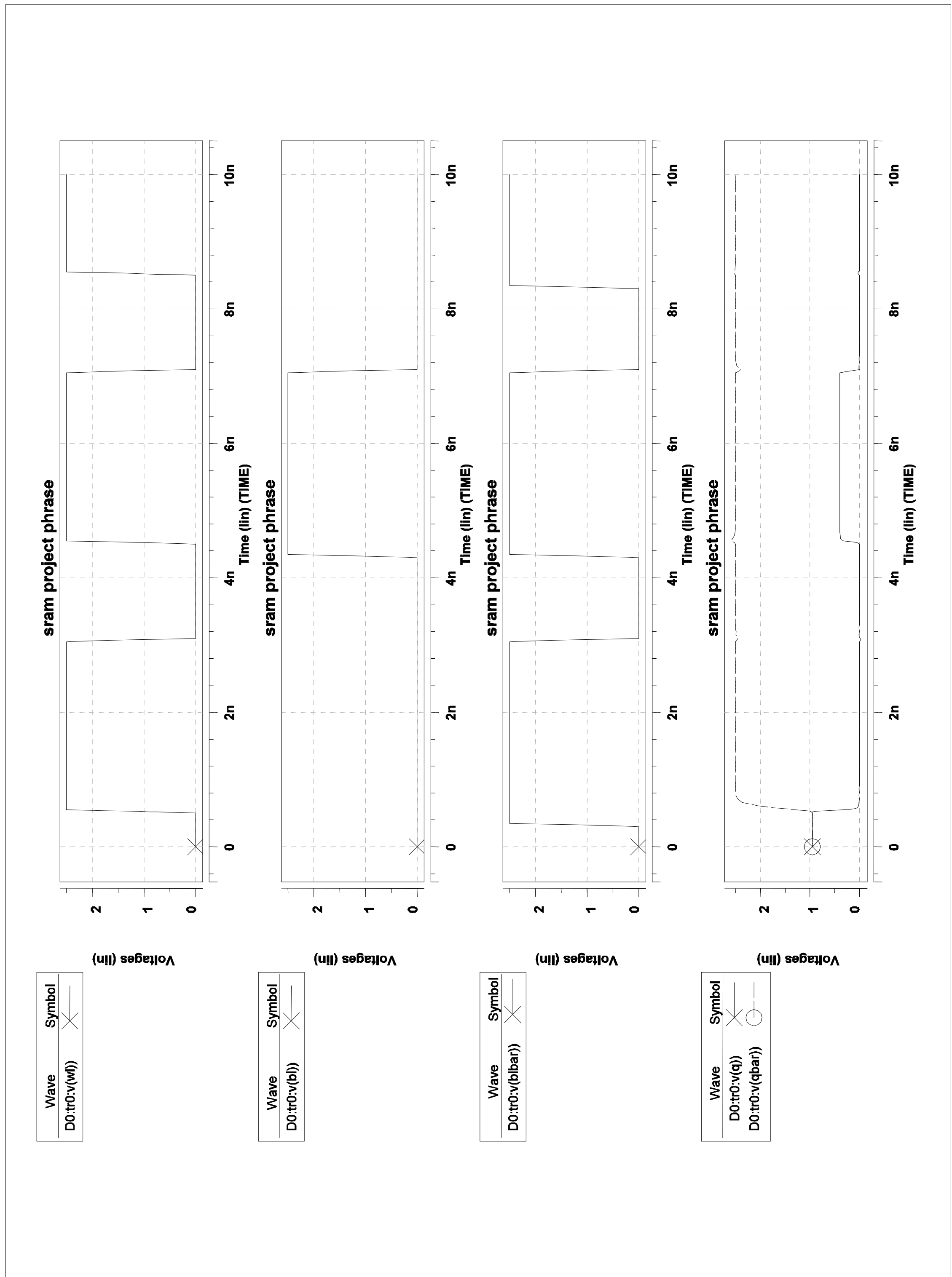

Figure 6 Write 0 to q followed by a read

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```
SRAM PROJECT PHRASE

.lib '/home/ff/ee141/MODELS/g25.mod' TT

*****************************************
* Parameter
*****************************************
.param vddp=2.5
.param vwl=2.5
.param vbl=0
.param vblbar=0
* find the optimal nmos width
.param w = 1.32
.param wpulldown='0.48u'
.param pmoswidth=0.36u
* increase the size of capacitance
.param cright=.5pF
.param cleft=.5pF

*****************************************
* Netlist
*****************************************
*M<name> <drain> <gate> <source> <bulk> <model> <geometry>
M1 qbar q 0 0       nmos l=0.24u w='wpulldown'
M2 qbar q vdd vdd  pmos l=0.24u w='pmoswidth'
M3 q qbar 0 0       nmos l=0.24u w='wpulldown'
M4 q qbar vdd vdd  pmos l=0.24u w='pmoswidth'
M5 qbar wl blbar 0 nmos l=0.24u w=0.36u
M6 q wl bl 0       nmos l=0.24u w=0.36u

VDD vdd 0 'vddp'
*VWL wl 0 'vwl'

* generate pulses for word line and bit lines. In the first cycle, write
* a zero to q; in the second cycle, read 0 from q
VWL wl 0 pulse(0 2.5 .5n 0.05n 0.05n 2.5n 4n)
VBLBAR blbar 0 pulse(0 2.5 .3n 0.05n 0.05n 2.7n 4n)
VBL bl 0 pulse(0 2.5 4.3n 0.05n 0.05n 2.7n 8n)

Cblbar blbar 0 'cleft'
Cbl bl 0 'cright'

*****************************************
* Analysis
*****************************************
.options post=2 nomod
.op

.tran 0.01ns 10ns *sweep w 1.08 1.8 .06
* In both scenarios, we want to check the maximum voltage at q
.meas q_max_wr max v(q) from=.6n to=3.5n
.meas q_max_rd max v(q) from=4.6n to=7.5n

.END
```

Transient Analysis with switch

```
SRAM PROJECT PHRASE

.lib '/home/ff/ee141/MODELS/g25.mod' TT

****************************************
* Parameter
****************************************
.param vddp=2.5
.param vwl=2.5
.param vbl=0
.param vblbar=0
* find the optimal nmos width
.param w = 1.32
.param wpulldown='0.48u'
.param pmoswidth=0.36u
* increase the size of capacitance
.param cright=.5pF
.param cleft=.5pF

****************************************
* Netlist
****************************************
*M<name> <drain> <gate> <source> <bulk> <model> <geometry>
M1 qbar q 0 0      nmos l=0.24u w='wpulldown'
M2 qbar q vdd vdd  pmos l=0.24u w='pmoswidth'
M3 q qbar 0 0      nmos l=0.24u w='wpulldown'
M4 q qbar vdd vdd  pmos l=0.24u w='pmoswidth'
M5 qbar wl blbar 0 nmos l=0.24u w=0.36u
M6 q wl vx 0       nmos l=0.24u w=0.36u

* syntax for ideal switch: G1 node1 node2 VCR PWL(1) node3 V Resistance
* V Resistance, where node3 is the controlling voltage. For example, the
* syntax below said that the switch is controlled by phi1; if it is 0V,
* the off resistance is 100Gohm; if it is 2.5V, the on resistance is 1uohm
G1 vx bl VCR PWL(1) phi1 0 0,100G 2.5,1u
*G2 vx 0 VCR PWL(1) phi1 0 0,100G 2.5,1u
* controlling voltage source
Vphi1 phi1 0 pwl(0 0 .4n 0 0.4000001n 2.5 4.4n 2.5 4.4000001n 0 )


VDD vdd 0 'vddp'
*VWL wl 0 'vwl'

* generate pulses for word line and bit lines. In the first cycle, write
* a zero to q; in the second cycle, read 0 from q
VWL wl 0 pulse(0 2.5 .5n 0.05n 0.05n 2.5n 4n)
VBLBAR blbar 0 pulse(0 2.5 .3n 0.05n 0.05n 2.7n 4n)
VBL bl 0 pulse(0 2.5 4.3n 0.05n 0.05n 2.7n 8n)

Cblbar blbar 0 'cleft'
Cbl bl 0 'cright'

****************************************
* Analysis
****************************************
.options post=2 nomod
.op

.tran 0.01ns 10ns *sweep w 1.08 1.8 .06
* In both scenarios, we want to check the maximum voltage at q
.meas q_max_wr max v(q) from=.6n to=3.5n
.meas q_max_rd max v(q) from=4.6n to=7.5n

.END
```