UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EECS 141: Digital Integrated Circuits - Spring 2006

Report Cover Sheet

TERM PROJECT: SRAM Design Cover Sheet

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Report 2 – Decoder design
Due Monday, April 3, 2006 by 10am in drop box.

Names
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Parameter	Value	Units
Decoder delay (estimate)	670.10	ps
Decoder delay (extracted)	664.45	ps
Wordline capacitance	12.60438	fF

	GRADE
Approach, result and correctness (60%)	
Report (40%)	
TOTAL	

Decoder Design

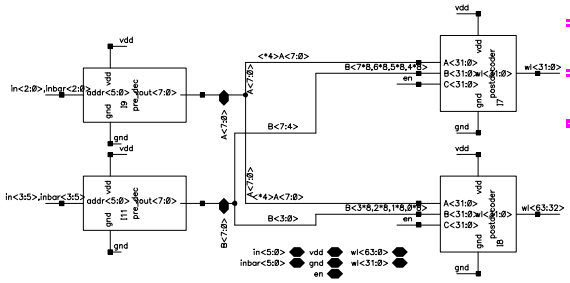


Figure 1: Decoder Schematic

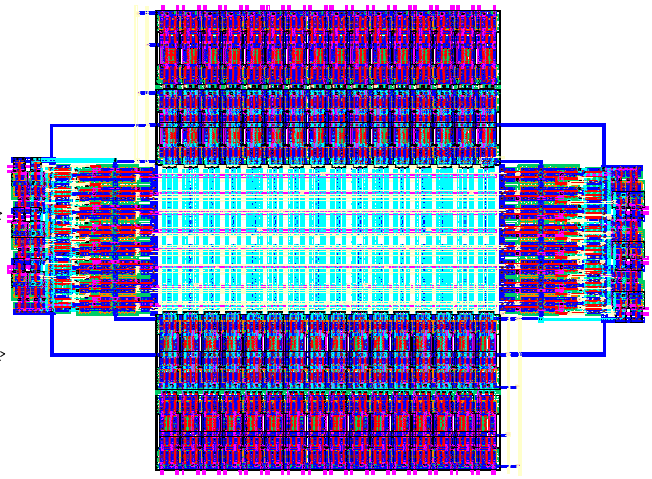


Figure 2: Cadence Decoder Layout

(left) Schematic of 6-to-64 decoder. 12 inputs (6 inputs with their complements) are decoded into 64 distinct wordlines. (right) The 6-inputs are placed on both the left and the right ends of the layout, and 32-outputs to the wordlines are placed on both the top and the bottom of the layout.

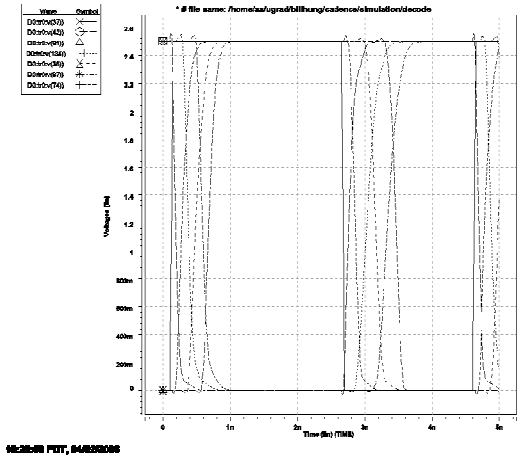


Figure 3: HSPICE Delay Simulation

Simulation

The worst case delay is 670.1ps.

tplhtot	tphltot	tptot	tplh1
5.604e-10	7.797e-10	6.701e-10	8.331e-11
tphl1	tp1	tplh2	tphl2
6.231e-11	7.281e-11	9.636e-11	9.553e-11
tp2	tplh3	tphl3	tp3
9.594e-11	1.795e-10	8.640e-11	1.330e-10
tplh4	tphl4	tp4	tplh5
1.191e-10	1.203e-10	1.197e-10	1.905e-10
tphl5	tp5	tplh6	tphl6
9.032e-11	1.404e-10	1.059e-10	1.107e-10
tp6	trise	tfall	
1.083e-10	1.888e-10	1.726e-10	

Expected Calculation

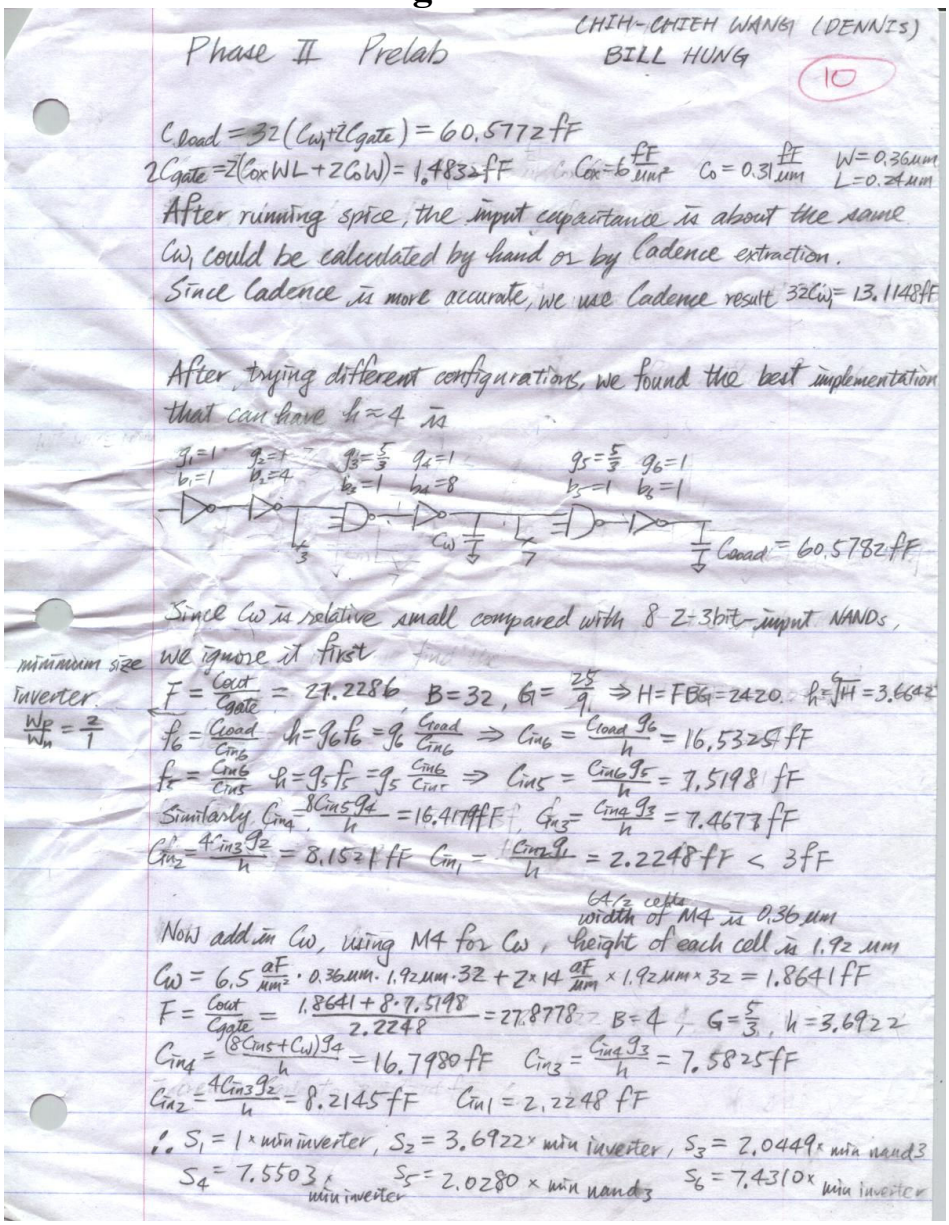
tphl = 19.77ps and tplh = 21.80ps, so tp = 20.79ps. According to the delay equation [Rabaey, 255]

$$D = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right) \text{ where } \gamma = 1$$

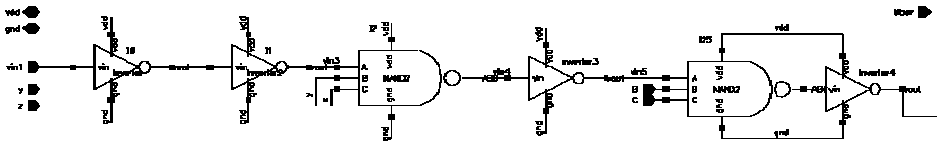
$D = t_{p0}(1+1+3+1+3+1+ 6 * 3.66) = 664.45\text{ps}$

Note that the simulated delay (670.1ps) is longer than the hand calculation (664.45ps) because many wiring capacitances were not considered in the hand calculations, but existed in simulation. In hand calculation, only capacitances from word lines were considered, capacitances due to branching wires and gates were ignored. In the simulation, each gate has larger load to drive, so the simulated delay is longer.

Hand Design of the Decoder



Wordline Capacitance = 12.60438 fF



We calculated the path effort, and we found that the optimal stages is 6 with the schematic above. In the layout we need to make the width and length to the closest multiple of lambdas. Therefore, the widths of pmos and nmos become the widths for PMOS and NMOS are listed below (from left to right of the schematic). Lengths are all minimum length 024um.

PMOS Width (um)= 0.72 2.64 1.5 5.4 1.44 5.34

NMOS Width (um)= 0.36 1.32 2.22 2.7 2.16 2.64

