

UNIVERSITY OF CALIFORNIA AT BERKELEY  
COLLEGE OF ENGINEERING  
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

## EECS 141: Digital Integrated Circuits - Spring 2006

### Report Cover Sheet

#### TERM PROJECT: SRAM Design Cover Sheet

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**Report 2 – Decoder design**

Due Monday, April 3, 2006 by 10am in drop box.

Names	
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Parameter	Value	Units
<i>Decoder delay (estimate)</i>	670.10	ps
<i>Decoder delay (extracted)</i>	664.45	ps
<i>Wordline capacitance</i>	12.60438	fF

	GRADE
Approach, result and correctness (60%)	
Report (40%)	
TOTAL	

## Decoder Design

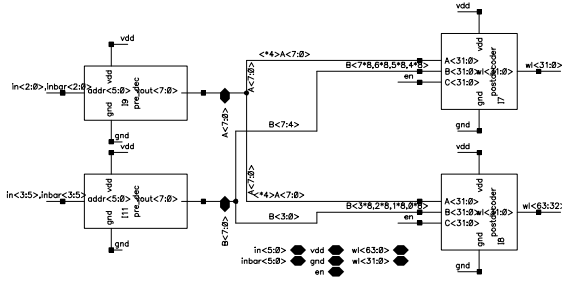


Figure 1: Decoder Schematic

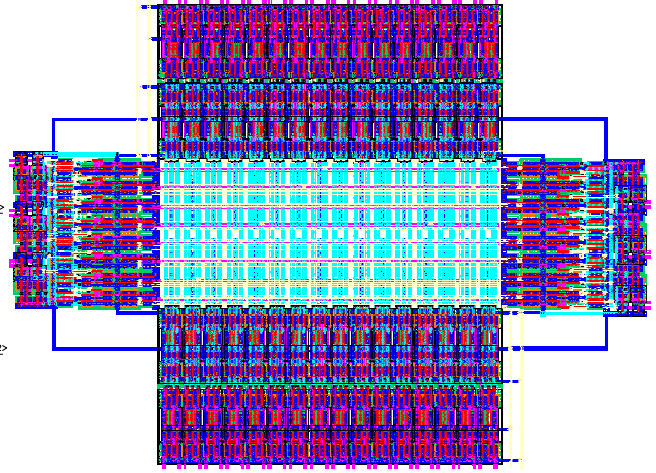


Figure 2: Cadence Decoder Layout

(left) Schematic of 6-to-64 decoder. 12 inputs (6 inputs with their complements) are decoded into 64 distinct wordlines. (right) The 6-inputs are placed on both the left and the right ends of the layout, and 32-outputs to the wordlines are placed on both the top and the bottom of the layout.

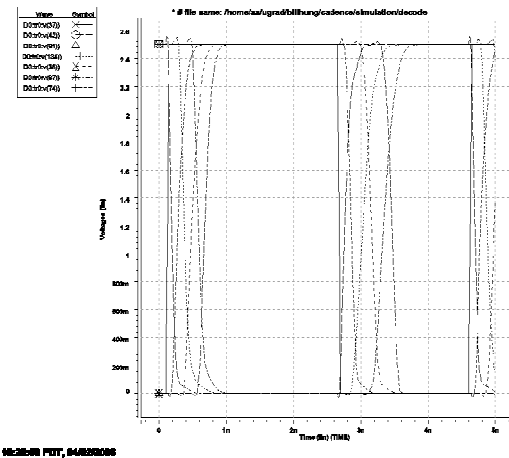


Figure 3: HSPICE Delay Simulation

### Simulation

The worst case delay is 670.1ps.

tplhtot	tplhtot	tptot	tplh1
5.604e-10	7.797e-10	6.701e-10	8.331e-11
tphl1	tp1	tplh2	tphl2
6.231e-11	7.281e-11	9.636e-11	9.553e-11
tp2	tplh3	tplh3	tp3
9.594e-11	1.795e-10	8.640e-11	1.330e-10
tplh4	tplh4	tp4	tplh5
1.191e-10	1.203e-10	1.197e-10	1.905e-10
tphl5	tp5	tplh6	tphl6
9.032e-11	1.404e-10	1.059e-10	1.107e-10
tp6	trise	tfall	
1.083e-10	1.888e-10	1.726e-10	

### Expected Calculation

$tplh = 19.77ps$  and  $tplh = 21.80ps$ , so  $tp = 20.79ps$ . According to the delay equation [Rabaey, 255]

$$D = t_{p0} \left( \sum_{j=1}^N p_j + \frac{N(\sqrt[N]{H})}{\gamma} \right) \text{ where } \gamma = 1$$

$$D = t_{p0}(1+1+3+1+3+1+6 * 3.66) = 664.45ps$$

Note that the simulated delay (670.1ps) is longer than the hand calculation (664.45ps) because many wiring capacitances were not considered in the hand calculations, but existed in simulation. In hand calculation, only capacitances from word lines were considered, capacitances due to branching wires and gates were ignored. In the simulation, each gate has larger load to drive, so the simulated delay is longer.

## Hand Design of the Decoder

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BILL HUNG

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Phase II Prelab

$$C_{load} = 32(C_{int} + C_{gate}) = 60.5772 \text{ fF}$$

$$2C_{gate} = 2(C_{ox}WL + 2C_GW) = 1.4832 \text{ fF}$$

After running spice, the input capacitance is about the same  $C_{in}$  could be calculated by hand or by cadence extraction.  
Since cadence is more accurate, we use cadence result  $32C_{in} = 13.1148 \text{ fF}$

After trying different configurations, we found the best implementation that can have  $h \approx 4$  is

Since  $C_{in}$  is relative small compared with 8 2-bit input NANDs, we ignore it first

minimum size inverter  $\frac{W_p}{W_n} = \frac{2}{1}$

$$F = \frac{C_{load}}{C_{gate}} = 27.2286, B = 32, G = \frac{25}{9} \Rightarrow H = F \cdot G = 2420, h = \sqrt[4]{H} = 3.6642$$

$$f_6 = \frac{C_{load}}{C_{in6}}, h = g_6 f_6 = g_6 \frac{C_{load}}{C_{in6}} \Rightarrow C_{in6} = \frac{C_{load} g_6}{h} = 16.5325 \text{ fF}$$

$$f_5 = \frac{C_{in6}}{C_{in5}}, h = g_5 f_5 = g_5 \frac{C_{in6}}{C_{in5}} \Rightarrow C_{in5} = \frac{C_{in6} g_5}{h} = 7.5198 \text{ fF}$$

Similarly  $C_{in4} = \frac{8 C_{in5} g_4}{h} = 16.4177 \text{ fF}, C_{in3} = \frac{C_{in4} g_3}{h} = 7.4678 \text{ fF}$

$$C_{in2} = \frac{4 C_{in3} g_2}{h} = 8.1521 \text{ fF}, C_{in1} = \frac{C_{in2} g_1}{h} = 2.2248 \text{ fF} < 3 \text{ fF}$$

Now add in  $C_{in}$ , using M4 for  $C_{in}$ , width of M4 is  $0.36 \mu\text{m}$ , height of each cell is  $1.92 \mu\text{m}$

$$C_{in} = 6.5 \frac{\text{aF}}{\mu\text{m}^2} \cdot 0.36 \mu\text{m} \cdot 1.92 \mu\text{m} \cdot 32 + 2 \times 14 \frac{\text{aF}}{\mu\text{m}^2} \times 1.92 \mu\text{m} \times 32 = 1.8641 \text{ fF}$$

$$F = \frac{C_{load}}{C_{gate}} = \frac{1.8641 + 8 \cdot 7.5198}{2.2248} = 27.8778, B = 4, G = \frac{5}{3}, h = 3.6922$$

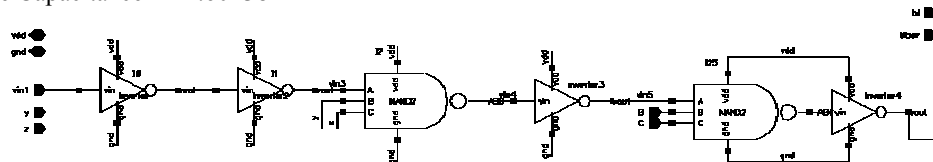
$$C_{in4} = \frac{(8 C_{in5} + C_{in}) g_4}{h} = 16.7980 \text{ fF}, C_{in3} = \frac{C_{in4} g_3}{h} = 7.5825 \text{ fF}$$

$$C_{in2} = \frac{4 C_{in3} g_2}{h} = 8.2145 \text{ fF}, C_{in1} = 2.2248 \text{ fF}$$

$\therefore S_1 = 1 \times \text{min inverter}, S_2 = 3.6922 \times \text{min inverter}, S_3 = 2.0449 \times \text{min NAND3}$

$S_4 = 7.5503 \times \text{min inverter}, S_5 = 2.0280 \times \text{min NAND3}, S_6 = 7.4310 \times \text{min inverter}$

Wordline Capacitance = 12.60438 fF



We calculated the path effort, and we found that the optimal stages is 6 with the schematic above. In the layout we need to make the width and length to the closest multiple of lambdas. Therefore, the widths of pmos and nmos become the widths for PMOS and NMOS are listed below (from left to right of the schematic). Lengths are all minimum length 0.24um.

PMOS Width (um)= 0.72 2.64 1.5 5.4 1.44 5.34

NMOS Width (um)= 0.36 1.32 2.22 2.7 2.16 2.64