Lab 8 D/A Conversion and Waveform Generation

Bill Hung
17508938
EE145M

Lab Time: 9-12pm Wednesday
Lab Partner: Chih-Chieh Wang (Dennis)
Station 13

Aim

Interface with a digital-to-analog (D/A) converter via LabView. The LabView VI generates both static DC voltage and time-varying waveforms. In this lab, a square wave and a triangular wave are generated. Finally, deviation between a linear model and the actual D/A output is measured.

1. Setup

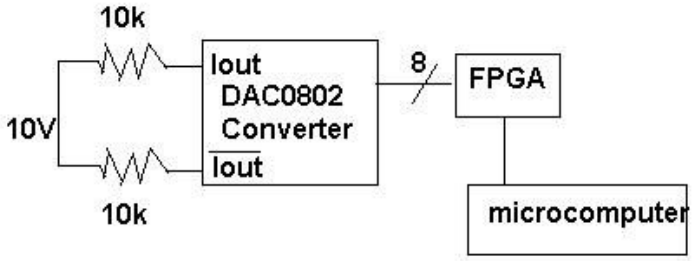
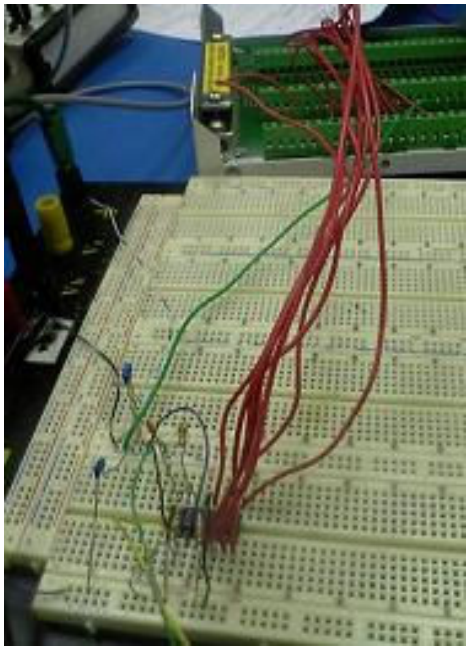


Figure 1.1. Setup Diagram

Datasheet from National Semiconductor - http://cache.national.com/ds/DA/DAC0800.pdf



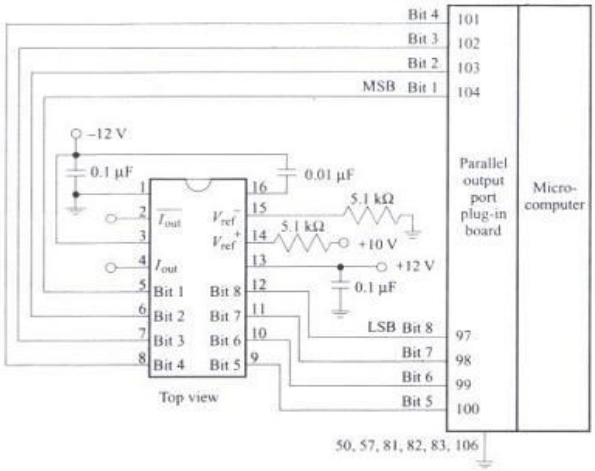


Figure 1.2.(Up) DAC 0802 Converter Pin Layout Diagram (Derenzo, 208, Figure 8.1). Two 10k resisters were connected to Iout and Iout-bar to measure the output current via a digital multimeter. Op-Amp was not used to amplify the output voltage. 10V reference voltage was used in the actual setup instead of 12V.

Figure 1.3. (left)Actual circuit setup. The green box was connected to the FPGA board. The FPGA green box is connected to the chip via the 8 digital bits (red wires). The chip used was a DAC 0802 converter chip.

2. Data summary

2.1 Comparison between measurements and the linear model. Summarize your results in a table.

Table 2.1-1. Comparing measurements and the linear model

n, step from n-1 to n	Vn, measured D/A output voltages (V)	Vlin(n), linear model (V)	Vn-Vlin(n), difference in millivolts	[Vn-Vlin(n)]/delta(V) in LSB
1	0.0973	0.0979	-0.6	-0.015306122
21	0.868	0.8819	-13.9	-0.354591837
41	1.6565	1.6659	-9.4	-0.239795918
61	2.4376	2.4499	-12.3	-0.31377551
81	3.2162	3.2339	-17.7	-0.451530612
121	4.7775	4.8019	-24.4	-0.62244898
151	5.9424	5.9779	-35.5	-0.905612245
181	7.1137	7.1539	-40.2	-1.025510204
241	9.4565	9.5059	-49.4	-1.260204082
255	10.0034	10.0547	-51.3	-1.308673469

Table 2.1-2. End-point voltages

Digital input	Analog output (V)
255	10.004
0	0.0587

The zero-offset-voltage = 0.0587V

Reference Voltage = 10V

The average step size is delta(V), which is also called the least significant bit (LSB) [Derenzo, 154], which is 0.0392V in this case. [Vn-Vlin(n)]/delta(V) is the ratio between the measured difference [Vn-Vlin(n)] and the LSB 0.0392V. As the data in Table 2.1-1 shows, the ratio between [Vn-Vlin(n)] and Delta(V) in LSB varies. The End-point voltages shown on Table 2.1-2 give information about the actual min/max voltages.

Sample Calculation for Linear Model.

Vlin(n) = delta(V)*n + voltage_min [Derenzo, 207]
= [0.0392] *n+0.0587

Vlin(255) = [0.0392] *255+0.0587
= 10.0547V

Sample Calculation for [Vn-Vlin(n)]/delta(V) in LSB

delta(V) in LSB = (Vref+ - Vref-)/n [Derenzo, 154]
= (10V-0V)/255
= 0.0392V

[Vn-Vlin(n)]/delta(V) = [0.868V - 0.8819V]/ 0.0392V
= -13.9mV/ 0.0392V
= -0.3546

2.2 RMS deviation. Compute the rms deviations Vrms between your data and the linear response given in the background section:

$$V_{rms} = \sqrt{\frac{1}{M}\sum_{i=1}^{M}[V^{lin}(n_i) - V_{ni}]^2}$$

where the summation is carried out only over your M measured values of V(ni). Note: Omit the end points in the summation since they are used to define the linear response and contribute zero.

Table 2.2. Vrms Calculation

Points	n, step from n-1 to n	Vn-Vlin(n), difference in millivolts	[Vn-Vlin(n)]^2
1	21	0.8819	0.00019321
2	41	1.6659	8.836E-05
3	61	2.4499	0.00015129
4	81	3.2339	0.00031329
5	121	4.8019	0.00059536
6	151	5.9779	0.00126025
7	181	7.1539	0.00161604
8	241	9.5059	0.00244036
		Vrms	0.02884909

A high Vrms means a large difference between the actual measurements and the ideal output voltage, and low Vrms means a small difference. **The Vrms is 0.02884V** in this case.

2.3 Differential Linearity. Tabulate Vn-V_n-1 from your measured data for several values of n. Estimate differential nonlinearity in units of LSB.

n, step from n-1 to n	Vn-Vlin(n), difference in millivolts	[Vn-Vlin(n)]/delta(V) in LSB
41	-0.0094	-0.239795918
61	-0.0123	-0.31377551
81	-0.0177	-0.451530612
121	-0.0244	-0.62244898
	average of [Vn-Vlin(n)]/delta(V)	-0.406887755

Delta(V) in LSB = 0.0392V.

Differential Linearity = -0.40689

Differential Linearity is the difference between the output step sizes and the average step size, which is usually expressed in units of 1 LSB. [Derenzo, 155] The Differential Linearity is -0.40689 in this case.

2.4 Power-supply rejection ratio
For n=0 and 255, compute the power-supply rejection ratio as delta(Vn)/delta(Vs), where delta(Vn) is the change in D/A output Vn for a power supply change delta(Vs).


Figure 2.4-1 10V V(255)


Figure 2.4-2 9V V(255)


Figure 2.4-3 10V V(0)


Figure 2.4-4 9V V(0)

Table 2.4 Power-supply rejection ratio

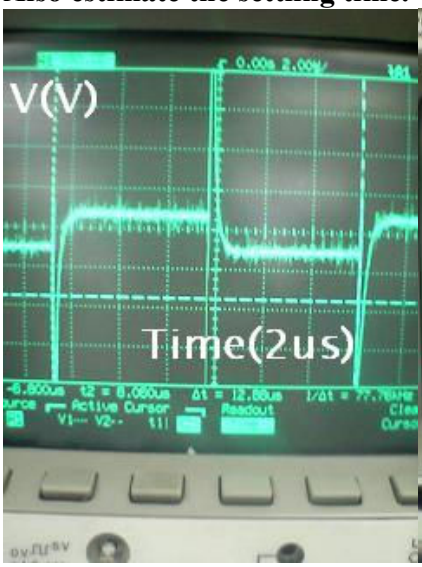
Digital Input	Analog output at 10V	Analog output at 9V	Delta(Vn) (V)	Delta(Vs) (V)	Delta(Vn)/Delta(Vs)
255	10.004	9.0033	1.0007	1	1.0007
0	0.0587	0.0514	0.0073	1	0.0073

First, a reference voltage of 10V was used. A digital input of 255 had an analog output of 10V, and input of digital 0 had an analog output of 0.059V.
Then, the reference voltage of 10V was reduced by 10% (=9V). A digital input of 255 had an analog output of 9V, and input of digital 0 had an analog output of 0.051V.

Power-supply rejection ratio is the percentage change in output voltage per 1% change in supply voltage [Derenzo, 155]. In other words, that is how much the DAC output changes if you change the supply voltage by 1. In this case, the maximum output voltage decreased proportionally with the decrease in supply voltage. Notice when the supply voltage was decreased from 10V to 9V, the output voltage was also decreased from 10V to 9V. That corresponds to a **delta(Vn)/delta(Vs) ratio of 1**. On the other hand, a decrease of supply voltage has almost no effect on the minimum output voltage. That corresponds to a **delta(Vn)/delta(Vs) ratio of 0.007**.

The delta(Vn)/delta(Vs) ratio presented is not accurate in this lab because the reference voltage was reduced from 10V to 9V. In the correct procedures, the reference voltage should not be decreased. The proper setup would reduce the Vsupply to 9V while keeping the Vref+ at 10V. Despite the error in lab procedures, the calculations were done in Table 2.4.

2.5 Glitch description. Include a sketch of the 127<->128 glitch you observed in procedure section 4. Label the voltage and time axes, and estimate the voltage and duration of the glitch. Also estimate the settling time.



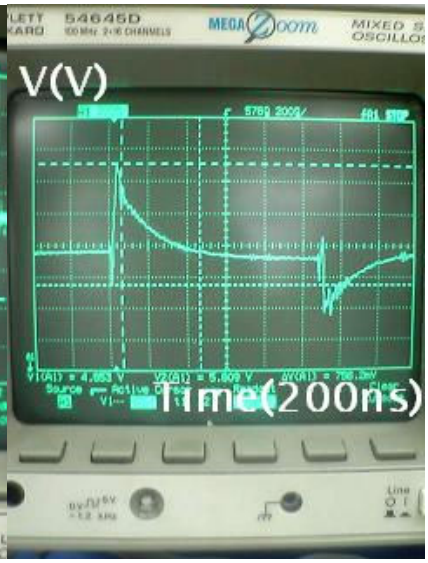
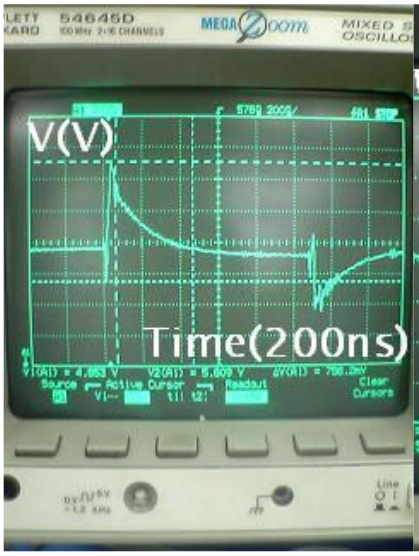


Figure 2.5-1 (left) n of 127-128 oscillating. The period measured as 12.86us as shown on the picture.
Figure 2.5-2 (right) n of 127-128 enlarged for amplitude measurement. Vpp of 756.2mV was shown.

As the output voltage oscillate between 127 and 128, a glitch was observed at the beginning of the transition. The glitch first "shoots up" to the maximum level, giving the **amplitude of the glitch to be 756.2mV**. **The duration of the glitch was measured to be 49ns**, which is the time of voltage change to the peak of the glitch. The period of the wave was 12.86us.



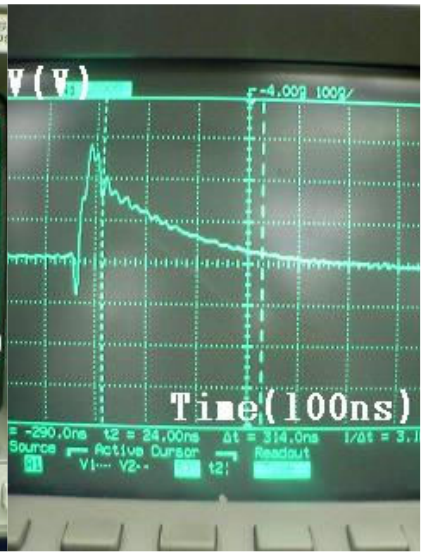
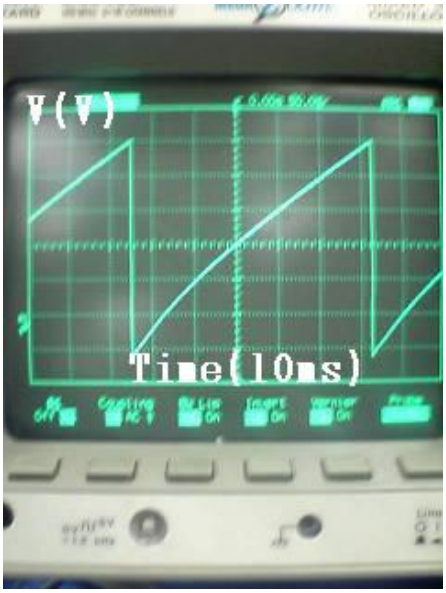


Figure 2.5-3 (left) Measuing Settling Time
Figure 2.5-4 (right) Measuing Settling Time in enlarged plot

The settling time measured was 399ns, which is about 4 times longer than the settling time suggested in the datasheet [National Semiconductor http://cache.national.com/ds/DA/DAC0800.pdf]. The settling time was measured from the time of the peak of the glitch to the time when the output voltage was stable.

2.6 Waveform generation. From your observations of the ramp waveform, compute the frequency that your program was able to send numbers to the D/A.



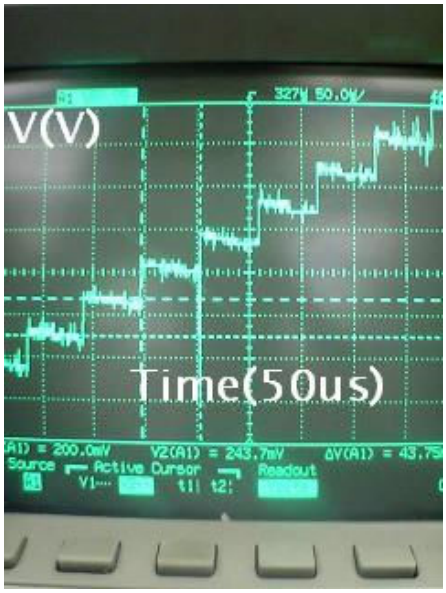


Figure 2.5-5 (left) Stepping waveform. Figure 2.5-6 (right) Stepping waveform enlarged.

A rising step waveform was generated to measure the step width and step height. **The step width was 56us and the step height was 43.75mV. The frequency the LabView program can send numbers to the D/A is 1/56us = 17.85 kHz.** The step height 43.75mV was a little off from the LSB calculation, 39.2mV, in section 2.1.

2.7 Generate other cyclic waveform

A triangular waveform was generated. The step width was still 56us and the step height was still 43.75mV. The frequency the LabView program can send numbers to the D/A is therefore still 1/56us = 17.85kHz .

3. Discussion

3.1 Discuss the importance of good power-supply rejection for D/A converters used in battery-operated equipment.

Having a good power-supply rejection for D/A converters give a more accurate measurements when the power supply is not stable enough. In other words, if the battery provides a 10V supply voltage, but if the actual supply voltage ranges from 9 to 11V, then the power-supply rejection ratio can tell how the D/A converter output changes. For example, a power-supply rejection ratio of 1 will gives a maximum DAC output ranges from 9 to 11V. The power-supply rejection ratio is important when the supply voltage from the battery is not stable enough. This is an important ratio to determine the effect of the supply voltage on the DAC output voltage.

3.2 Discuss the case of the glitches observed in procedure section 4 in terms of the operation of the D/A converter.

The D/A converters are a collection of current switches. Each switch is responsible for outputting certain amount of current. The glitch is a transient spike while the digital bit changes. When the digital bit that is controlling the analog output changes, the internal switches within the D/A converter do not change simultaneously. For a short period of time, the digital input has a different value from the intended digital input. Therefore, the analog output has the wrong voltage value for that short period of time. When the digital input settles, the analog output will also settles to a constant value after some delay.

3.3 Discuss the relative accuracy and the differential linearity measured in procedure section 5.

Relative Accuracy is the difference between the measured transition voltages V(n, n+1) and a straight line passing from the first to the last transition voltage [Derenzo, 163]. This accuracy can adjust to zero-offset (Vmin) of the experimental setup, because the relative accuracy depends on the transitions of the smallest (n, n+1) and the largest (n, n+1) pairs. The mathematical representation of the ideal value is:

$$V^{lin}(n,n+1) = V_{0,1} + n\left(\frac{V_{2^N-2,2^N-1} - V_{0,1}}{2^N - 2}\right)$$

=0.0973V + n(10.0034-0.0973)/254

=-41.0mV (Table 3.4-1)

Differential Linearity is the difference between the output step sizes and the average step size, which is usually expressed in units of 1 LSB. [Derenzo, 155] The LSB, the least significant bit is the average step size [Derenzo, 154], which is 0.0392V in this case. The Differential Linearity is -0.40689 in this case. In other words, the difference between the output step sizes and the average calculated average step size is about 0.40689 times the LSB.

The accuracy was also calculated as Vrms in procedure section 5(section 2.2 of the report) Mathematically, the Vrms is defined as:

$$V_{rms} = \sqrt{\frac{1}{M}\sum_{i=1}^{M}[V^{lin}(n_i) - V_{ni}]^2}$$ [Derenzo,2100].

The ideal linear model values differ from the measured experimental values as shown in Table 2.2. Taking all the differences between the ideal values and the measured values, an average Vrms is calculated. A high Vrms means a large difference between the ideal values and the measured values. If the Vrms is low, then the measured values better match the ideal values. In this lab, the Vrms is 0.02884V.

3.4 Describe how the properties you measured for your D/A differ from the datasheet specifications in terms of relative accuracies, differential linearity, glitch amplitude, settling time, and power-supply sensitivity. Note that not all useful properties may be found in the data sheets.

Relative Accuracy is the difference between the measured transition voltages V(n, n+1) and a straight line passing from the first to the last transition voltage [Derenzo, 163]. The mathematical representation of the ideal value is:

$$V^{lin}(n,n+1) = V_{0,1} + n(\frac{V_{2^N-2,2^N-1} - V_{0,1}}{2^N - 2})$$

=0.0973V + n(10.0034-0.0973)/254

Table 3.4-1 Relative Accuracy

n	Vn, measured D/A output voltages (V)	ideal value	relative accuracy
1	0.0973	0.136300394	-0.039000394
21	0.868	0.916308268	-0.048308268
41	1.6565	1.696316142	-0.039816142
61	2.4376	2.476324016	-0.038724016
81	3.2162	3.25633189	-0.04013189
121	4.7775	4.816347638	-0.038847638
151	5.9424	5.986359449	-0.043959449
181	7.1137	7.15637126	-0.04267126
241	9.4565	9.496394882	-0.039894882
255	10.0034	10.04240039	-0.039000394
		average	-0.041035433

Average Relative Accuracy=-41.0mV

Table 3.4-2 Comparisons between measured and Datasheet values

	Measured	Datasheet
Relative Accuracy	-41.0mV	+- 1LSB=39.2mV
Differential Linearity	-0.407	N/A
Glitch Amplitude	756.2mV	N/A
Settling Time	399ns	100ns
Power-Supply Sensitivity	0.7300%	0.0001%

I could not find any information about glitch amplitude and differential linearity in the datasheet. The measured glitch amplitude is 756.2mV, and differential linearity is -0.40689. For relative accuracy, I took the full scale error from the datasheet +-39.2mV, which seems to be a close comparison to the measured value -41.0mV.

The measured settling time 399ns was 4 times longer than the datasheet value of 100ns. This may be due to the different definition of settling time. The settling time of the measured value measures the time from the peak of the glitch to the time when the output voltage is stable. The datasheet value for power-supply sensitivity is 0.0001%, which does not match the measured value of 0.73%. This is because the procedure error mentioned in section 2.4. The measured value shown in Table 3.4-2 was taken from the digital input 0, which shows a lower power-supply sensitivity value.

4. Questions

4.1 How would errors in the reference voltages affect the absolute accuracy and relative accuracies of the D/A?

Relative Accuracy is the difference between the measured transition voltages V(n, n+1) and a straight line passing from the first to the last transition voltage [Derenzo, 163]. The mathematical representation of the ideal value is:

$$V^{lin}(n,n+1) = V_{0,1} + n(\frac{V_{2^N-2,2^N-1} - V_{0,1}}{2^N - 2})$$

=0.0973V + n(10.0034-0.0973)/254

Average Relative Accuracy = -41.0mV (see Table 3.4-1)

Absolute Accuracy is the difference between the measured input transition voltages V(n, n+1) and their ideal values V(n, n+1)[Derenzo, 163]. The mathematical representation of the ideal value is:

$$V(n,n+1) = Vref^{-} + (n+\frac{1}{2})(\frac{Vref^{+} - Vref^{-}}{2^N - 1})$$

=(n+1/2) (0.0392V)

Table 4.1 Absolute Accuracy

n	Vn, measured D/A output voltages (V)	ideal value	absolute accuracy
1	0.0973	0.0588	0.0385
21	0.868	0.8428	0.0252
41	1.6565	1.6268	0.0297
61	2.4376	2.4108	0.0268
81	3.2162	3.1948	0.0214
121	4.7775	4.7628	0.0147
151	5.9424	5.9388	0.0036
181	7.1137	7.1148	-0.0011
241	9.4565	9.4668	-0.0103
255	10.0034	10.0156	-0.0122
		average	0.01363

Average Relative Accuracy = 13.6mV

The error in reference voltage will not affect the relative accuracy because the relative accuracy depends on the actual transitions. However, the error in reference voltage will increase the absolute accuracy because the absolute accuracy depends on ideal values that are independent of measured values.

4.2 What was the maximum milli-volt deviation between your observed D/A output and the linear model?

51.3mV.

4.3 How would you use a sample and hold amplifier to remove the glitches?

I would connect the output of the D/A (which had the glitch) to a sample and hold amplifier and connect the sample and hold amplifier to a "valid data" signal so that it is in hold mode when “valid data” is false. [Derenzo, midterm review Slides 15] In our Lab 8, we can have a counter that is activated each time we change the digital input. The counter will wait for certain interval before generating the "valid data" signal. The resulting analog signal is slightly delayed but glitch free.

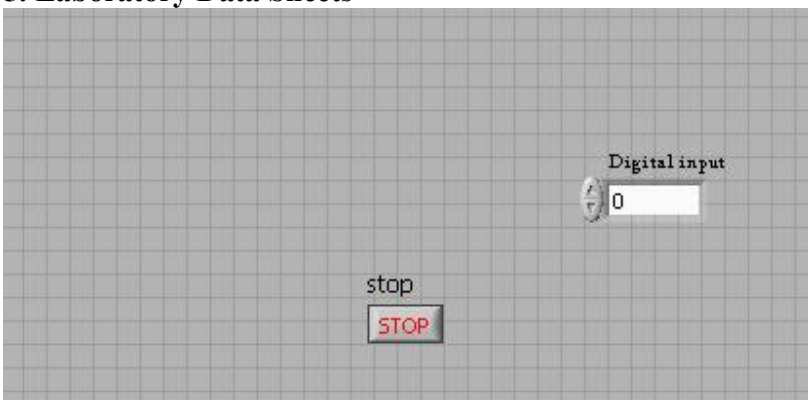
4.4 Based on the measured settling time between 7Fh and 80h transitions, what is the maximum conversion rate of the D/A converter? Which factor is the first to place an upper bound on the maximum conversion rate, the D/A converter or the speed of the I/O port? Justify your answer.

The glitch duration + settling time = 49ns+399ns = 448ns. The maximum conversion rate is 1/448ns = 2.23MHz. However, the speed of the I/O port put an upper bound on the maximum conversion rate, because the I/O port operates in the order of microseconds. Because of the speed of the I/O port, the actual maximum conversion rate was 17.85 kHz (see section 2.6).

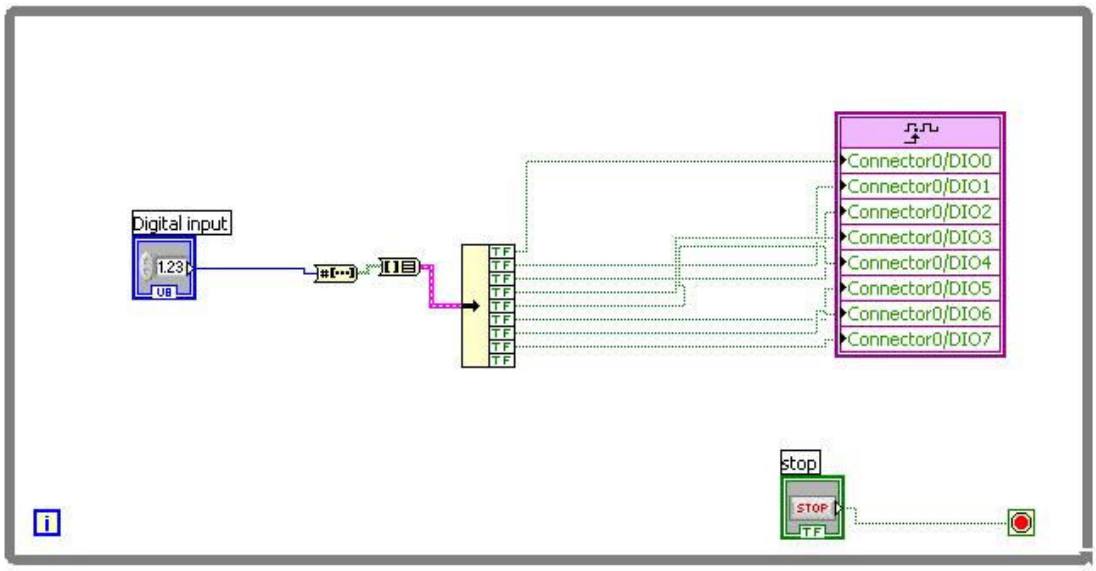
4.5 Arbitrary waveforms can be generated by interfacing a D/A converter with dedicated logic (an FPGA board) or a software controlled I/O port (on a computer). What are the advantages of a FPGA driven waveform generator over a waveform generator driven directly by software? When would a software based system be preferable? Consider voltage accuracy, maximum frequency, system interrupts, glitches and flexibility.

The FPGA board operates at least 10 times faster than a software driven waveform generator. The result is FPGA has a faster maximum frequency, and the glitches are less severe because the switches can switch faster. The software driven waveform has various system interrupts at the high level software side, which introduce delays and errors into the measurements. Thus, software driven waveform generator tends to be less accurate. However, the software driven waveform generator offers a higher flexibility because data is usually stored directly on the computer, and data can be easily manipulated by a computer program. A software based system is preferred when the budget is low, because a FPGA board is not needed for D/A conversion. The software based system is also preferred when high flexibility is desired.

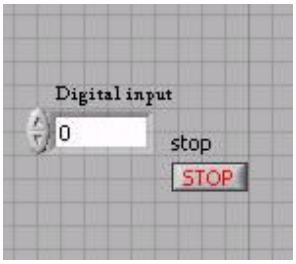
5. Laboratory Data Sheets



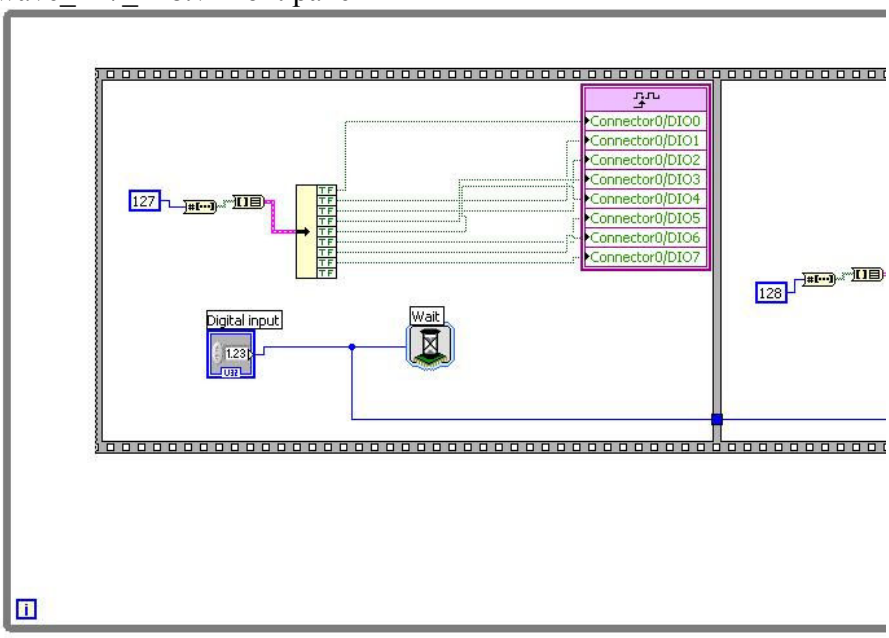
DAC.vi Front Panel. This VI responsible for the static waveform.

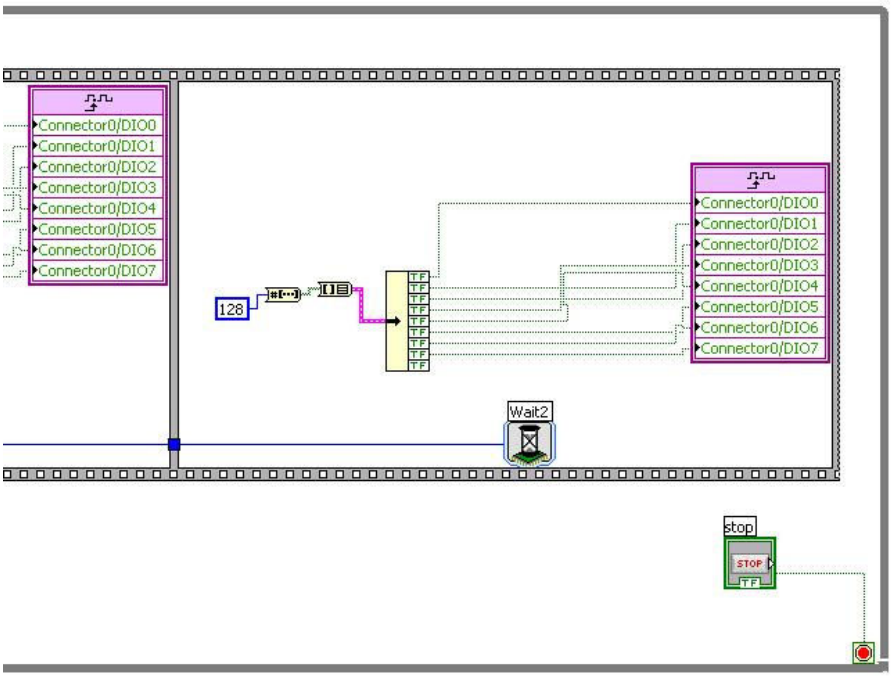


DAC.vi Block Diagram. The unsigned 8-bit number goes through a cluster, then unbundled to 8 true-or-false array. The true-or-false values are output to 8 pins on the FPGA board. The LabView program continues to run until the stop button ends the while-loop.

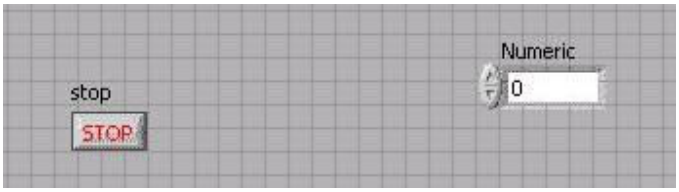


wave_127_128.vi front panel

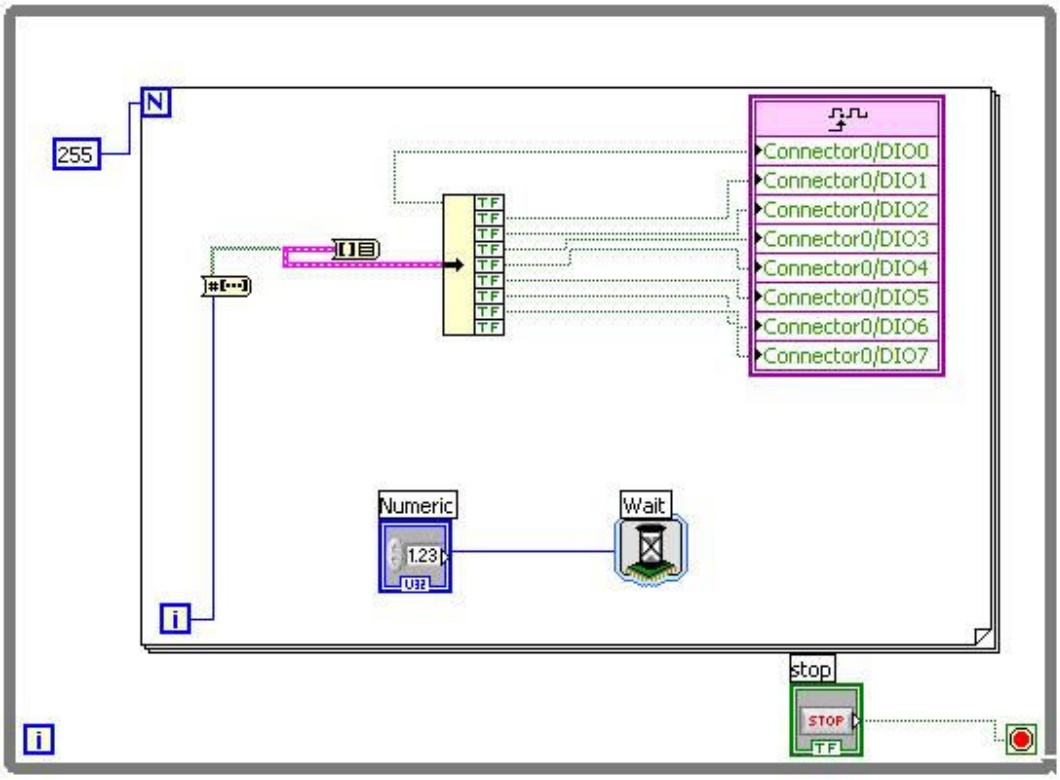




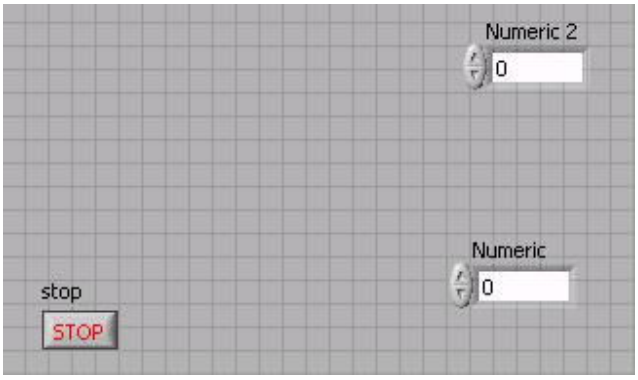
wave_127_128.vi block diagram. The 2 frames generates 127 and 128 alternatively.



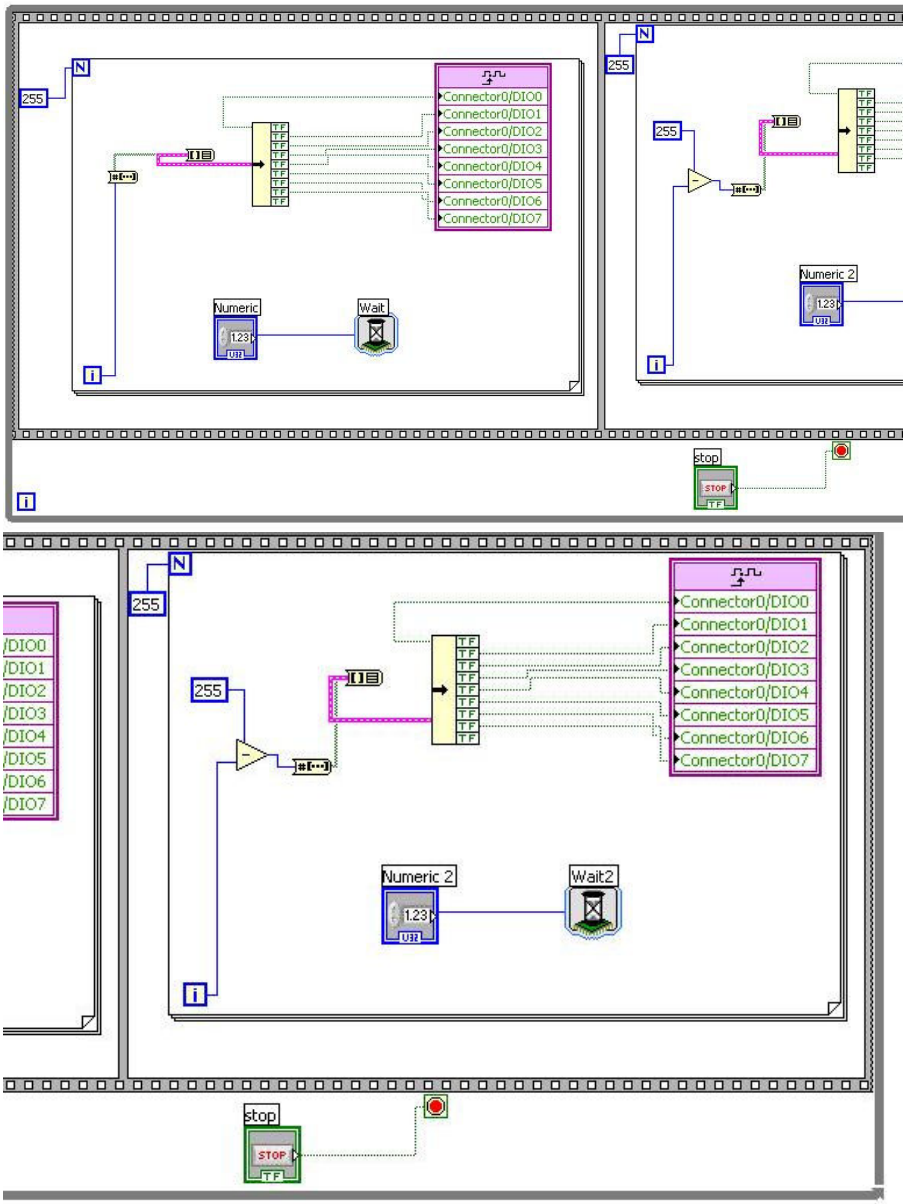
ramp.vi front panel



ramp.vi block diagram



triangular.vi front panel



triangular.vi block diagram. The voltage increases, then decreases.